A 45 dB Variable Gain Low Noise MMIC Amplifier

M. Anowar Masud*, Herbert Zirath*,#, Matthew Kelly*

* Chalmers University of Technology, Microwave Electronics Laboratory, 412 96 Gothenburg, Sweden

Ericsson AB, Microwave and High Speed Research Center, 431 84 Mölndal, Sweden

***Abstract* — A variable gain amplifier operating at 2.5 GHz based on Single Ended topology has been designed and characterized. Three such stages were cascaded preceded by a single stage LNA. A source follower is used at the output as an active load matching. Overall dynamic gain variation is 45 dB with a maximum gain of 47 dB. The -3 dB bandwidth is 0.800 GHz. A minimum noise figure of 0.81 dB is obtained in the highest gain mode. Maximum value of 1 dB compression at the output is -7.2 dBm and the corresponding third order intercept point is +5.3 dBm. Consumed DC power 285 mW and is immune to gain variation. The circuit is implemented with GaAs pHEMT technology. The combined area occupied by the multistage low noise VGA and the single ended VGA is 3.5 mm X 3 mm.**

I. INTRODUCTION

A Variable gain amplifier is a versatile function block for radio communication and radar. It is used for controlling the transmitted signal power or adjusting the received signal amplitude in order to keep the signal to the detector constant. Our purpose is to design a controllable gain stage in the IF block of a 60 GHz WLAN demonstrator by cascading several stages of VGA following an LNA. There are usually four types of VGAs. (1) Current steering technique: The Gilbert Cell topology [1], [2] (2) Variable transconductance topology [3], [4] (3) Using an attenuator (dynamic/discrete) in conjunction with the amplifier [5], [6] (4) Feed back topology (both series and shunt) [7].

Apart from these conventional topologies, a folded cascode topology can be adopted for achieving a variable gain amplifier [8]. In a sub-micron CMOS technology, the gate of the PMOS is governed by the control signal to achieve the required gain variation.

II. THEORY-SOURCE FEED BACK TOPOLOGY

In the single ended VGA topology, the gain variation is achieved by varying the source resistance connected in feedback configuration in a typical small signal amplifier as shown in fig. 2. The small signal gain of an amplifier at low frequency can be written as:

$$G_n = -\frac{g_m R_d}{1 + g_{ds}(R_s + R_d) + g_m R_s} \text{----------(1)}$$

For a typical HEMT g_{ds} is usually small, equation (1) can therefore be approximated as:

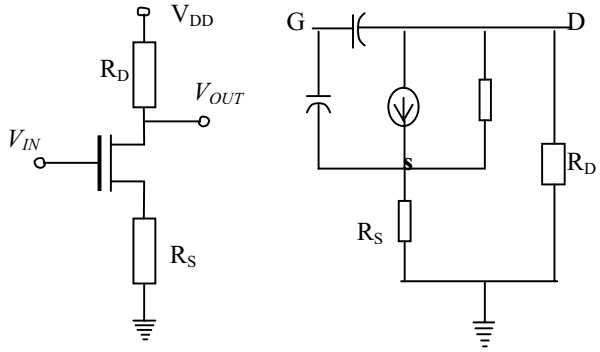


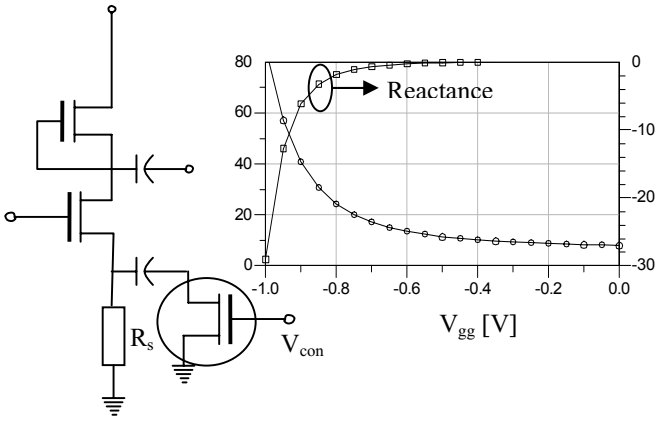
Fig. 1. (a) Source feedback amplifier (b) Simplified small signal equivalent circuit

$$G_n = -\frac{g_m R_d}{1 + g_m R_s} \approx -\frac{g_m R_d}{g_m R_s} = -\frac{R_d}{R_s} \text{-----(5)}$$

By changing the source resistance, it is possible to control the gain of the amplifier in a practical way. As far as the operation of the VGA is concerned in the low frequency region i.e. at 2.5 GHz, the gain is inversely proportional to the source resistance.

Variation of the source resistance is achieved by connecting the drain terminal of a HEMT in zero bias mode (without any drain bias) in parallel to the source resistance by a bypass capacitor. The source terminal of the HEMT is grounded. A variable DC voltage at the gate is used to govern the channel resistance (Fig. 2). To

maximise the gain an active load with a size of 2 X 15 μm transistor is used at the drain [Fig. 2(a)]. Three such stages are cascaded preceded by an LNA. Finally, the output is taken from a source follower. Used bias for the circuit is 4 Volts at the drain and 1 Volt at the gate network. The common source LNA with inductive source feed back uses a bias of 2.5 V at the drain and



(a) (b)

Fig.2. (a) VGA schematic with the control transistor connected to the source through a by pass capacitor (b) Variation [simulated] of small signal impedance with the gate excitation

-0.6 V at the gate. Size of the transistor size used in the LNA is 4 X 100 μm. Fig. 3 shows a single stage VGA cascaded with a source follower. Size of the corresponding transistors has also been mentioned in the adjacent table. The source follower is designed in constant current source self bias mode. It uses a supply of 2.7 volts at the drain. It has two advantages:

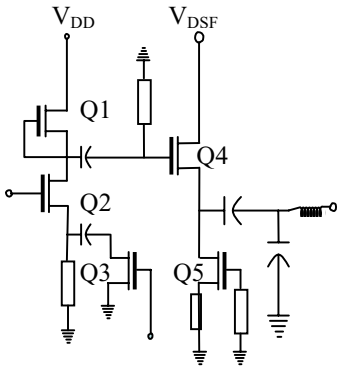


Table:I

Comp	Size (μm)
Q_1	2 X 15
Q_2	4 X 50
Q_3	4 X 50
Q_4	2 X 25
Q_5	2 X 15

Fig 3. A single stage VGA coupled with a source follower.

firstly, it provides active matching to the output port with proper scaling of the transistors (Q4 & Q5 in Fig. 3). Secondly, it isolates the load from the input. With the above source feed back topology, the VGA obtains high value of transconductance (g_m) ensuring better control of gain by the source resistor with high dynamic variation. Tansistor, Q2, is biased at (0.93, -0.85) with a sconductance (g_m) of 0.067 S. One of the advantages of this topology is the independence of bias point with control signal. The bias position of the active transistor (Q2) in the IV curve remains stable. This makes the dissipated power constant throughout the gain variation. Possibility of driving the transistor in the triode region during the gain swing is also obviated by this arrangement. VGAs implemented with gate control (dual gate) topology can suffer from this limitation if not maintained properly.

A commercial foundry, WIN of Taiwan, has been used for circuit fabrication. Model of the active device (pHEMT) was provided by the same foundry. The f_t of the transistor is 85 GHz, the maximum transconductance is 495 mS/mm and the pinch-off voltage is -1 Volts. The transistor used has a gate length of 0.15 μm with mushroomed shape in order to reduce the gate resistance. The break-down voltage is 10 Volts.

III. CIRCUIT IMPLEMENTATION AND PERFORMANCE

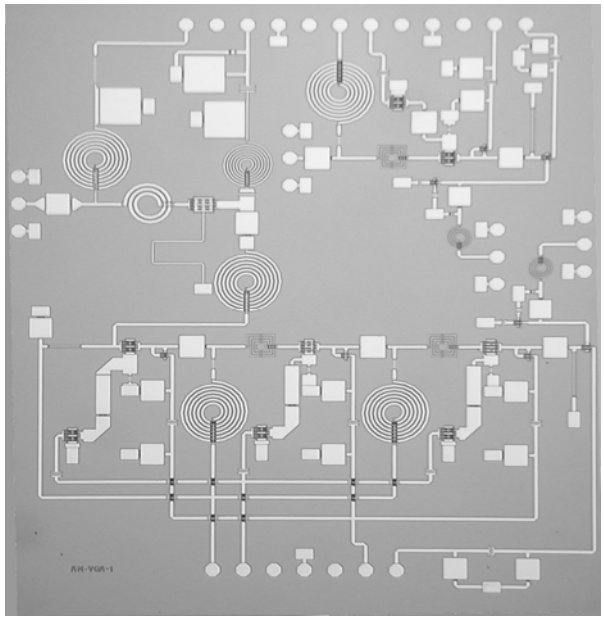


Fig 4. Micro-Photograph of the multistage VGA.

Fig. 4 shows the micro-photograph of the circuit on a chip size 3 X 3.5 mm coupled with LNA and source follower (SF). For proper utilization of the die area, a three stage VGA and a single stage VGA have been put on the same chip area. Both the multistage and a single stage VGA have been accommodated on the same chip for better utilization of the vacant die areas. Necessary decoupling networks have been used in all the bias paths in order to avoid oscillations. We are interested in the measurement of scattering parameters, noise figures, power compression, third order intercept point (TOI) of the given amplifier. For the VGA, variation of $|S_{21}|$ against control voltage is of prime importance. An Agilent PNA has been used to measure the S-Parameters while the noise figure (NF) was measured with an Agilent 8974A with HP 346C noise source. To measure the Power compression and the TOI, an Agilent 4419B power meter & Agilent 8565E spectrum analyzer have been used.

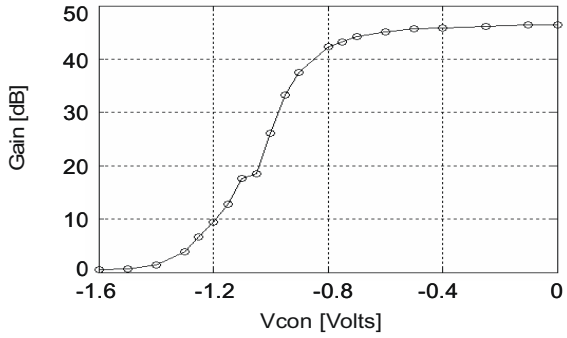


Fig 5. Variation of Gain with the control signal

Fig. 5 shows the variation of gain ($|S_{21}|$) with the control signal. The same information is conveyed by Fig. 6 in which the gain plotted against frequency with the control voltage as parameter.

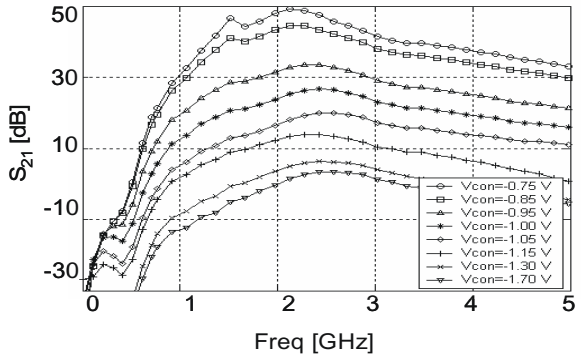


Fig 6. $|S_{21}|$ vs Frequency with the control voltage as parameter

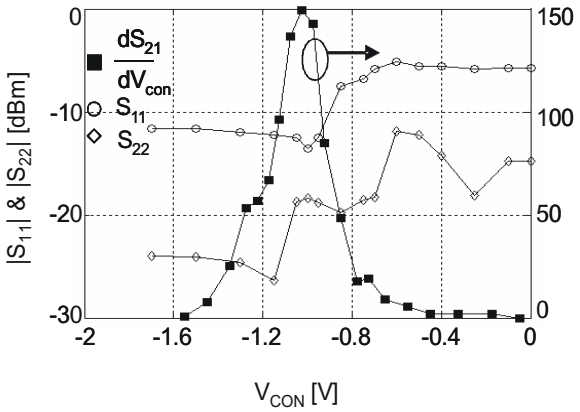


Fig 7. Rate of change of $|S_{21}|$ and reflection coefficient against V_{con}.

As evident from Fig. 2, with the increase of control voltage the amplifier gain increases because of the increase of overall source feed back impedance [Fig. 2(b)]. Fig. 7 shows the rate of gain variation with the control signal. Maximum value is found at V_{con}=-1 Volt [approx.]. On the same plot dependence of the reflection co-efficients on the control voltage has also been shown.

Noise Figure (NF) of the overall circuit is shown in figure Fig. 8 both against frequency (highest gain mode) and the control voltage. A minimum value of 0.82 dB is obtained at 2.5 GHz with an applied control voltage of zero volts. the NF remains constant (at around 0.85) as long as the control voltage remains above -1 volt. The compression characteristics is shown in Fig. 9. The minus one dB compression point at the output is -7.35 dBm and the TOI is +6.2 dBm (referred to the output).

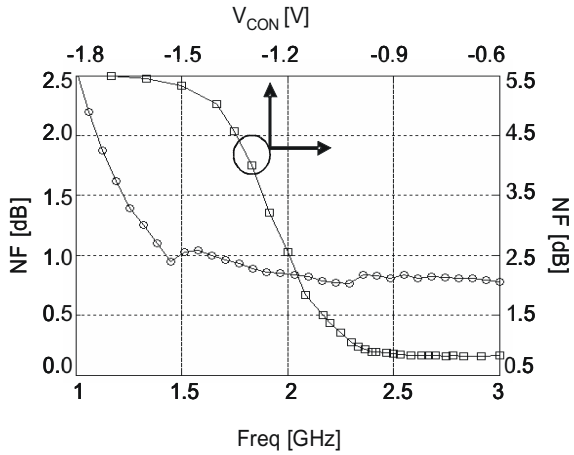


Fig 8. Noise Figure (NF) as a function of frequency and the control voltage, V_{con}.

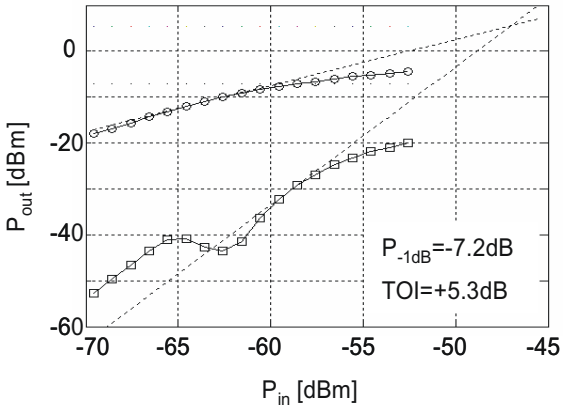
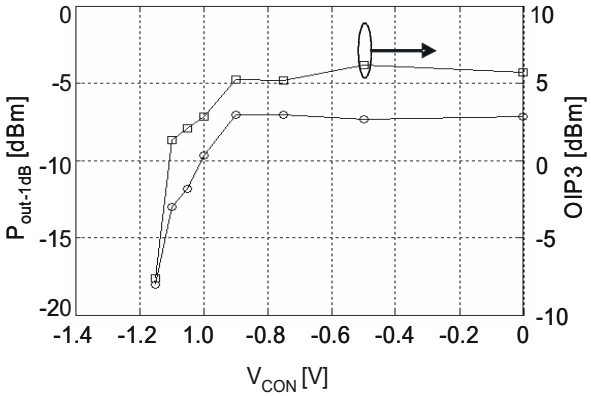


Fig 9 Compression characteristics in the maximum gain mode

The one dB compression point and the TOI even though remains constant, show some dependency on the control voltage variation.



This is shown in figure 10. The dependence is noticeable beyond -1 V of the control voltage.

IV. COMPARISON WITH THE PUBLISHED WORK

VGA reported in [3] claims gain margin of 8 dB with Max. gain at 16.8 dB. No information on IM3 or dependence of S_{11}, S_{22} on gain variation is provided in the paper. Same is true for the work [4] though here, the achieved gain variation is 16 dB. Work done in [6] claims a gain variation of 40 dB with Max. Gain of 18 dB. Also claim made by the author about the immunity of S_{11} on gain variation is incorrect. This can easily be shown by a simple derivation about the dependence of S_{11} on the control resistance. Considering the above, the reported work is comparatively better.

V. DISCUSSION AND CONCLUSION

A compact VGA-block based on variable resistive source series feedback using channel resistance of a HEMT, is designed, fabricated and verified experimentally. Maximum variation of gain at 2.5 GHz is 45 dB with a control voltage variation range of 1.5 volts. Maximum rate of variation is 150 dB/V at a control voltage of -1 V. Minimum noise figure is less than 1 dB in the highest gain mode.

VII. ACKNOWLEDGEMENT

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REFERENCES

[1] S. Aggarwal, A. Khosrowbeygi, A. Daanen, “A single-stage variable-gain amplifier with 70-dB dynamic range for CDMA 2000 transmit applications”, *IEEE Journal of Solid-State Circuits,* vol. 38, no. 6, pp. 911–917, 2003.

[2] R Saito, K. Hosoda, A. Hyogo, T. Maruyama, H. Komuraki, H. Sato, K. Sekine, “ A 1.8-V, 73-dB dynamic-range CMOS variable gain amplifier”, *ESSCIRC 2004-29th European Solid-State Circuits Conference*, pp. 301–314, 2003.

[3] Y. S. Wang, L. -H. Lu, “5.7 GHz low-power variable-gain LNA in 0.18 µm CMOS”, *Electronics Letters*, vol. 41, no. 2, pp. 66 –68, 2005.

[4] Q. Chaudhry, R. Alidio, G. Sakamoto, T. Cisco, “ A SiGe MMIC variable gain cascode amplifier”, *IEEE Microwave and Wireless Components Letters*, vol. 12, no. 11, pp. 424 –425, 2002.

[5] K. R. Nary, R. L. Van-Tuyl, “ An MMIC amplifier for automatic level control applications”, *IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium. Digest of Papers*, pp. 73-76, 1990.

[6] M. Detratti, J. P. Pascual, M. L. De-La-Fuente, J. Cabo, J. L. Garcia, “A GaAs monolithic linear-in-dB wide-dynamic-range variable-gain amplifier with matching compensation for 1.95-GHz applications”, *Microwave and Optical Technology Letters*, vol. 44, no. 3, pp. 251 – 257, 2005.

[7] K. Nishikawa, T. Tokumitsu, “An MMIC low-distortion variable-gain amplifier using active feedback”, *IEEE Transactions on Microwave Theory and Techniques*, vol. 43, no. 12, pt. 2. pp. 2812-2816, 1995.

[8] T. Ming-Da, L. Ren-Chieh, L. Chin-Shen, W. Huei, “A low-voltage fully-integrated 4.5-6 GHz CMOS variable gain low noise amplifier”, *Proceedings, 33rd European Microwave Conference*, vol. 1, pp. 13-16, 2003.