A Medium-Power Low-Noise Amplifier For X-Band Applications

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***Abstract* — A monolithic front-end amplifier for X-band radar applications has been developed utilising conventional low noise GaAs technology. The application requires low noise figure, high output power, good input and output return loss, high gain and reduced chip area. To simultaneously fulfil such conflicting requirements, proper design methods have been adopted. Measured results from 8.5 to 9.6 GHz demonstrate a noise figure lower than 1.5 dB, a small-signal gain of 29 dB, input and output return loss over 20 dB, with an associated output power at -1 dB gain compression in excess of 17 dBm.**

I. Introduction

GaAs MMIC technology is finally providing high yield and reliability performances and consequently it is widely adopted for the realisation of circuits and subsystems for microwave and millimetre wave apparatuses. Low noise amplifiers are key components of many microwave systems, requiring high-sensitivity front-end circuits, as in radar, satellite communication systems and radio-astronomy receivers [1]-[2]. Nevertheless, the low-noise characteristic is often accompanied to high output power performances, as in the case of radar receivers. The latter components must exhibit an high dynamic range, given the large potential variation of their inputs (-10 dBm is a typical upper limit). As a consequence, the design of the front-end amplifier involves design problems concerning the use of a low-noise technology to realise a circuit having good performances in terms of output power, together with adequate input and output return loss.

In this contribution, the design of a medium power low noise X-band amplifier operating in the 8.5 –9.6 GHz band, trying to trade off among the abovementioned requirements, is described. Design charts allowing the simultaneous control of the noise figure, input return loss and available gain have been utilised to design the input stage of the circuit. Moreover, properly designed lumped-element quadrature hybrid has been implemented to achieve the required output power and return loss performances with an acceptable increase in die area. Experimental results are illustrated to validate the design approach.

II. Circuit Design

The circuit has been designed using a 0.25 μm GaAs PHEMT technology from UMS. It is composed by three amplifying stages, each designed to fulfil one or more circuit specifications [3]. The first low noise stage has been designed to determine the noise figure and the input return loss of the circuit, while the second one actually controls the gain amplitude and the frequency response of the overall chain; the final stage is a medium power amplifier, designed to achieve the required output power and return loss.

Design charts allowing the simultaneous control of noise figure, gain and input return loss of an amplifier including a single active device have been generated to design the first stage. In fact, if the input and output matching network are reciprocal and lossless and the output port of the transistor is conjugately matched, the design is completely controlled by the input transistor termination (Γ_S); in particular, a well-defined relation exists between the available gain (G_{av}) of the stage and the magnitude of the reflection coefficient at the input of the overall stage (Γ) [5]-[6]:

$$|\Gamma|^2 = 1 - 2k \cdot \left|\frac{S_{12}}{S_{21}}\right| \cdot G_{av} + \left|\frac{S_{12}}{S_{21}}\right|^2 G_{av}^2 \quad (1)$$

where S_{ij} and k are the S parameters and the stability factor of the transistor respectively. Under the previous hypotheses, constant $|\Gamma|$ and G_{av} loci are coincident circle families in the Γ_S plane.

The transistor selected for the first stage has a 200 μm total gate periphery and it is biased at V_{DS}=2 V, at 20 % I_{DSS}. In such bias condition the transistor is conditionally stable over the full X-Band (k=0.2 and MSG=15.5 dB at 9.05 GHz). Device stability has been assured utilising biasing networks and a source series inductive feedback. To trade off among the stage performances, a design chart has been generated using the previously cited approach, with the feedback inductance value as a parameter. In such chart, depicted in Fig. 1, the minimum

noise figure of the stage that can be attained for a given available gain (NFMin, [4]) and the input return loss of the stage (IRL) are plotted as a function of G_{av} for three feedback inductance values. The curves refer to a stabilised device (k>1 after inductive feedback), characterised by an IRL monotonously increasing with G_{av}. The above chart, that can be automatically generated by means of a commercial CAD tools, clearly evidences the available trade-off solutions. For the selected value of the feedback inductance, a design chart on the Γ_S plane, including constant circles of available gain, input return loss and noise figure of the transistor, has been generated (Fig. 2). Such chart has been used to select the Γ_S corresponding to the desired trade off among the stage performances.

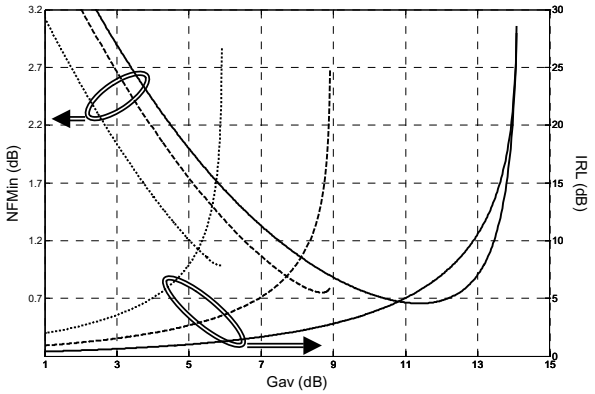

Fig. 1. NFMin and IRL of the first stage versus G_{av} at Ls=0.1 nH (solid), Ls=0.28 nH (dashed), Ls=0.55 nH (dotted).

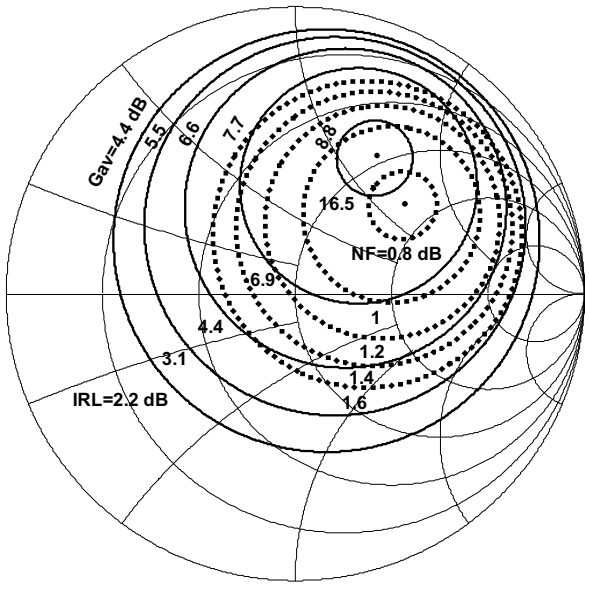

Fig. 2. Γ_S plane design chart for the first stage of the circuit.

To achieve the required output power and return loss, the third stage of the circuit has been designed utilising a balanced configuration, as shown in Fig. 3. The stage is composed by a pair of 50 Ω quadrature hybrids splitting the signal outgoing from the second stage and combining the outputs of two 200 μm devices biased at V_{DS}=3 V and 50 % I_{DSS} utilising a self-bias scheme. To achieve reduction in chip area, the quadrature hybrids have been designed using lumped-elements techniques [7]. They are composed of a lumped elements Wilkinson splitter and two lumped-elements phasing networks, each connected to its output ports, as shown in Fig. 4. The 90° phase difference between the hybrid outputs is achieved designing each phasing network to exhibit an insertion phase of ±45°; to this purpose they are synthesised with a third-order Chebyshev network [8].

The layout of the overall amplifier, having a die area of 3.7 X 2.3 mm^2, is shown in Fig. 5.

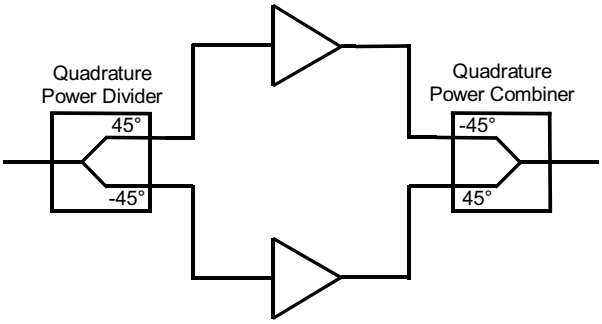

Fig. 3. Block scheme of the third stage of the circuit.

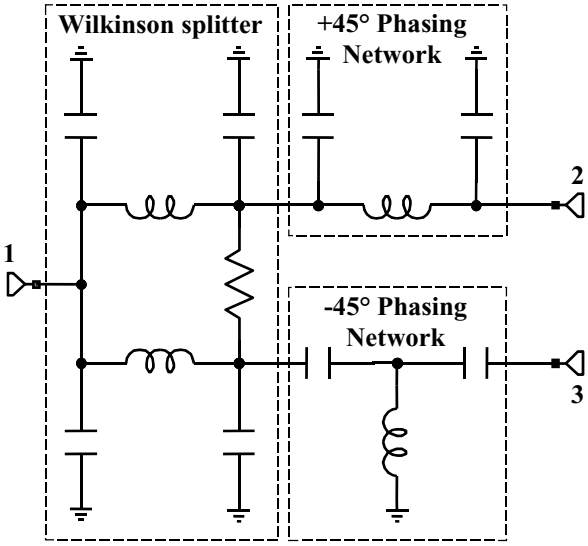

Fig. 4. Principle scheme of the realised lumped elements hybrid.

III. Measured Performance

S-parameters, noise figure and output power of the realised amplifier have been measured on wafer in the 8-10 GHz band. The resulting gain and noise figure performances are depicted in Fig. 6, demonstrating a small-signal gain of 29 dB with a ±0.2 dB ripple and a noise figure lower than 1.5 dB over all the design bandwidth. Measured input and output reflection coefficient magnitudes are plotted in Fig. 7: an input and output return loss greater than 20 dB result, thus confirming the outcome of the generated design charts.

Output power and large-signal gain are plotted in Fig. 8 as a function of the input drive level, an output power at -1 dB gain compression in excess of 17 dBm results.

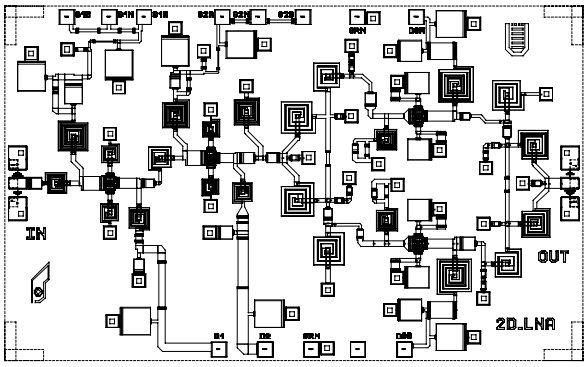

Fig. 5. Layout of the circuit.

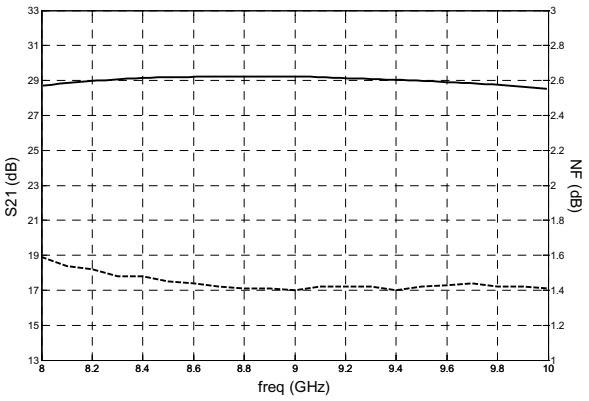

Fig. 6. Measured small signal gain (solid line) and noise figure (dashed line) of the circuit.

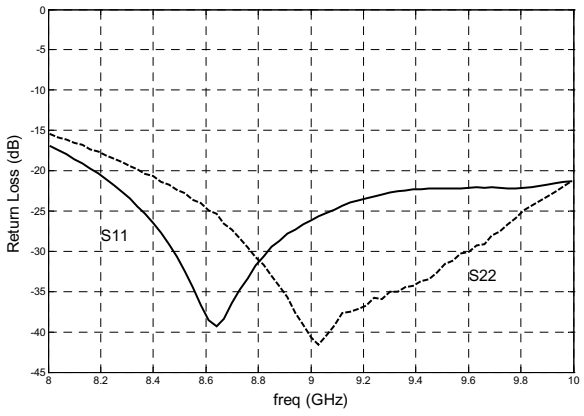

Fig. 7. Measured magnitude of the input and output reflection coefficients of the circuit.

IV. CONCLUSION

A X-band medium-power low-noise monolithic amplifier has been realised using a 0.25 μm low noise PHEMT GaAs technology by UMS. Proper design techniques have been utilised to achieve both low-noise and high output power performances together with high gain and high input and output return loss. Measured results confirm the validity of the utilised design approaches.

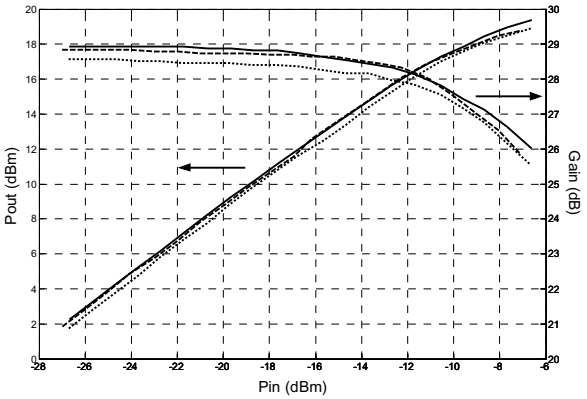

Fig. 8. Measured output power and large signal gain versus input power at 8.5 GHz (solid), 9.05 GHz (dashed), 9.6 GHz (dotted).

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