An Highly Integrated Double Conversion Mixer MMIC for Ka-band VSAT Communication Systems

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***Abstract* — For use as up-converter in Ka-band VSAT outdoor units, an highly integrated mixer with a double input for balanced operation was designed. This self-bias double conversion mixer MMIC has been designed in order to ease the integration, reduce the size, and finally reach the cost requirements for such systems. The mixer is a multifunction chip, which integrates two frequency doublers and a cold FET mixer for a chip size of only 2.88 mm^2. Such a compactness was achieved thanks to a 0.25-µm Pseudomorphic-HEMT process using MIM capacitors over via holes. The mixer exhibits broadband performance, with up-converter loss of only 8 dB for an LO power of +10 dBm and 10-GHz IF frequency.**

I. Introduction

The development of interactive multimedia services like telephone, high speed internet access, television broadcast, audio and video conferencing, requires data transmission at higher and higher rates. For these applications, the use of broadband wireless systems at millimeter wave frequencies offers interesting, fast and cost effective solutions for indoor and outdoor, professional and consumer applications like Point-to-Point, Point-to-Multi-Point, and VSAT (Very Small Aperture Terminals) [1]. However in these systems, the MMIC chipset represents of big fraction of the overall outdoor unit cost. Apart from the driver and power amplifiers, a VSAT power line-up requires a large number of sub-function MMICs like doublers, buffer amplifiers and the mixer itself [2]. Considering GaAs area as the main driving cost for MMICs, we present in this paper the performance of a broadband single chip double conversion mixer MMIC addressing especially the Ka-band VSAT application in the 29.5-30 GHz frequency band. This single chip, self-bias up-converter MMIC replaces nearly up to five MMICs within a chip area of only 2.9 mm^2. This represents a reduction by at least a factor of three in the amount of GaAs area required to achieve the same functions, which allows significant reduction in module complexity, assembly, filtering and cost.

II. Circuit Design

The MMIC technology is based on a standard 0.25µm PHEMT process (UMS PH25) on 100-µm 4'' GaAs substrates, using microtrip lines. As shown in Fig. 1, and Fig. 2, the single-chip mixer MMIC is a multifunction chip integrating two self-biased frequency doublers, isolated with buffer amplifier stages, and a cold FET mixer.

A cost effective chip set can be mainly achieved by an high level of compaction, because at constant yield, the MMIC cost is almost linear with GaAs area. By mean of advanced key design approaches using MIM capacitors over vias [3], and an higher chip complexity, it was possible to design such a compact double conversion mixer, which consists of only one MMIC within a die area of less than 2.9 mm^2.

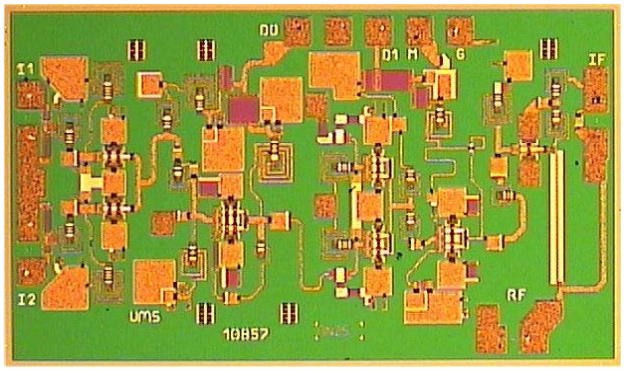

Fig. 1. Chip photograph of the double conversion mixer MMIC (chip size is 2.31 × 1.25 mm^2).

As shown in Fig. 2, the MMIC topology consists in an LO input frequency of 5.7 GHz doubled twice up to 22.8 GHz, then mixed with IF frequency band (6.7 GHz-7.2 GHz), resulting in signal operating in the 29.5 GHz- to 30 GHz frequency range.

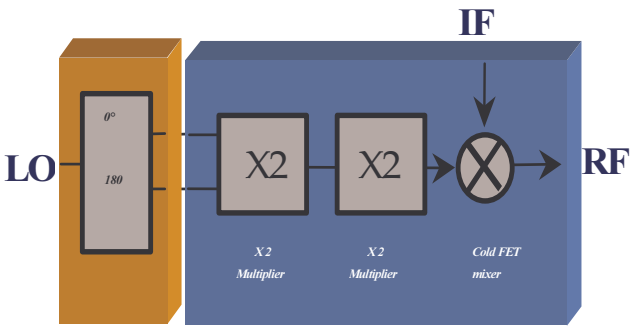

Fig. 2. Schematic of the double conversion mixer MMIC.

During the development phase, the first stage frequency doubler, the second stage frequency doubler, and the mixer were designed and tested separately.

A. 6-12GHz frequency doubler MMIC

The MMIC topology is based on a first stage doubler working as a balanced multiplier, followed by a 10- to 15 GHz one-stage buffer amplifier. The fundamental local oscillator frequency can be supplied by external Balun coupler. It is worth mentioning that the doubler can be operated in single ended mode as well.

A first issue in frequency doubler design is the choice of the gate-to-source bias, V_{gs}. The frequency doubler is constrained to operate near the pinch-off-region. By varying the source and the load impedance under DC bias condition, we calculated the highest possible second harmonic output with the fundamental output of the HEMT kept as minimum.

The external balun topology improves the fundamental rejection on the output by splitting the input signal with opposite phases and combining them on multiplier's output through a simple in-phase combiner. The balanced configuration was considered because it provides efficient rejection of the fundamental and the odd-harmonics. The typical on-wafer performances are described in Fig. 3. Especially, the second harmonic output power is better than +14 dBm for an output frequency between 10- and 16 GHz. Over the same frequency range, for the balanced configuration, the fundamental output power is lower than –10 dBm, resulting in a fundamental rejection better than 24 dBc.

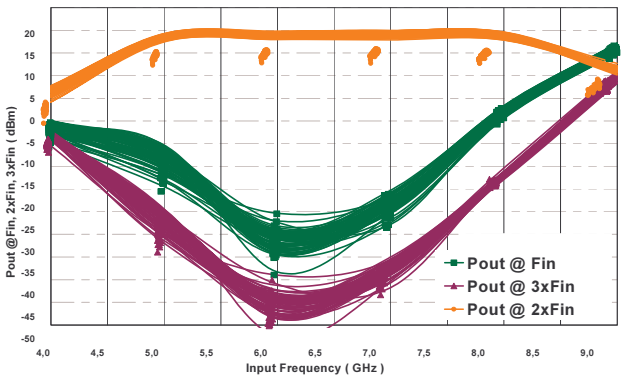

Fig. 3. On wafer measurement of the 6-12GHz frequency multiplier MMIC. Conversion loss and isolation versus input frequency. Frequency doubler tested in balanced mode, V_{ds}=3.5 V, I_{ds}=60 mA, Input power=10 dBm per input.

The same frequency doubler has been tested in single-ended mode. The second harmonic output power is nearly the same as balanced mode. However, in single-ended mode, the frequency doubler achieves the 14dBc fundamental rejection over a slightly reduced bandwidth, i.e.5-7 GHz.

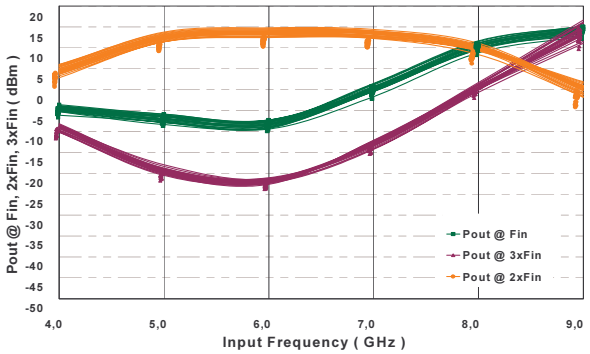

Fig. 4. On wafer measurement of 6-12GHz frequency multiplier. Conversion loss and isolation versus input frequency. Frequency doubler tested in single mode, V_{ds}=3.5 V, I_{ds}=60 mA, Input power=10 dBm per input.

B. 12-24GHz frequency doubler + mixer

The topology of the frequency multiplier is typically the same as first frequency doubler detailed previously. This one is based on a first stage working as the multiplier followed by a 20-30 GHz one stage buffer amplifier. All transistors are self biased.

The mixer is based on cold FETs structures. The benefit is to avoid any drain voltage supply and so to simplify the DC supply design. Good inter-modulation performance of this transmitter is achieve by using a resistive FET mixer, where the nonlinear output conductance at a drain-source voltage of 0 V is exploited for mixing. In Fig. 5, it is shown that for an LO input signal of 11.5GHz and an IF frequency varying between 1 GHz, and 10 GHz, the mixing circuit based on the frequency doubler, and the cold FET mixer achieves a conversion loss bellow than 8 dB at 5.7 GHz.

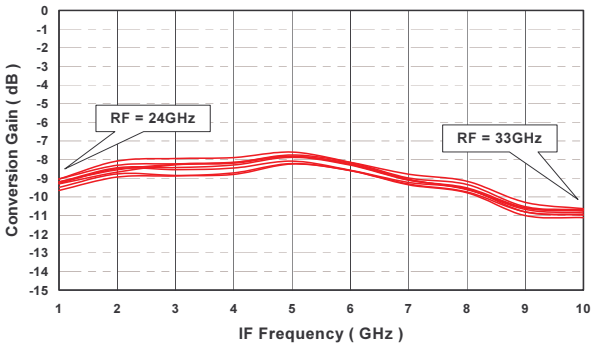

Fig. 5. X2 Multiplier + Mixer. Conversion loss versus IF frequency. F_{LO}=11.5 GHz, P_{LO}=+12 dBm, V_{ds}=3.5 V, I_{ds}=60 mA.

C. Double conversion mixer

Because of the high IF, the image is far away from the VSAT Ka-band, which ease the spurious filtering. The mixer can be used in single- or balanced local oscillator mode, by using an external 0-180° hybrid coupler for up-conversion. The main characteristics for the mixer MMIC are summarized in Table I.

TABLE I.

RF Frequency range (GHz)	22..37 GHz
IF Frequency range (GHz)	1..10 GHz
Conversion loss (dB)	< 9 dB
LO input power (dBm)	+10 dBm
IF Input Power at 1-dB gain compression	+8 dBm
DC Power Consumption:	100 mA @ 4 V

Fig. 6 shows the conversion loss and LO leakage (4 × LO) versus the LO frequency for a constant IF frequency of 6 GHz. At 5.7-GHz LO, the conversion loss are 8 dB, and the 4 × LO level is below -3 dBm.

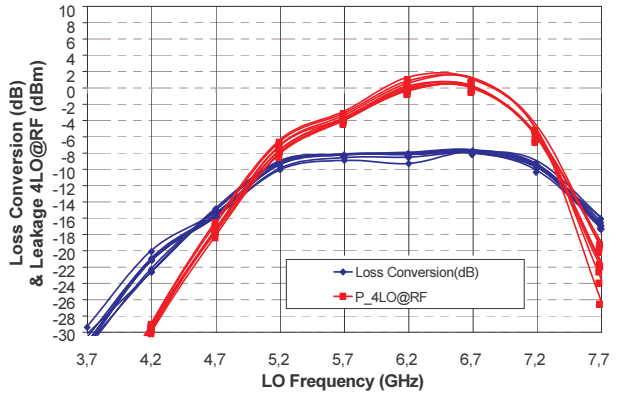

Fig. 6. Conversion loss and isolation versus LO-frequency and constant IF-frequency of 6 GHz.

Fig. 7 shows the conversion loss and LO leakage (4 × LO) over a broad IF frequency range (1 GHz to 10 GHz); the isolation is below –3 dBm and the conversion loss better then 8 dB, especially over the IF band used for the VSAT radio (6.7 GHz-7.2 GHz).

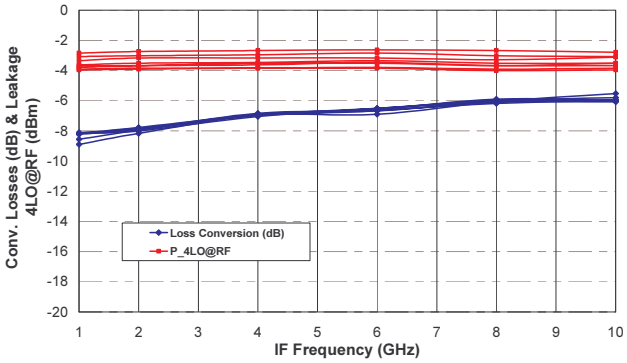

Fig. 7. Conversion loss and isolation versus IF-frequency and constant LO-frequency of 5.7 GHz.

The power characteristics are depicted in Fig. 8, and 9. The conversion loss as a function of IF input power at 10-dBm LO drive is presented for two different LO frequencies (F_{LO}=3 GHz, and F_{LO}=5.7 GHz). As shown in the input P-1dB compression point is between 8- and 11 dBm.

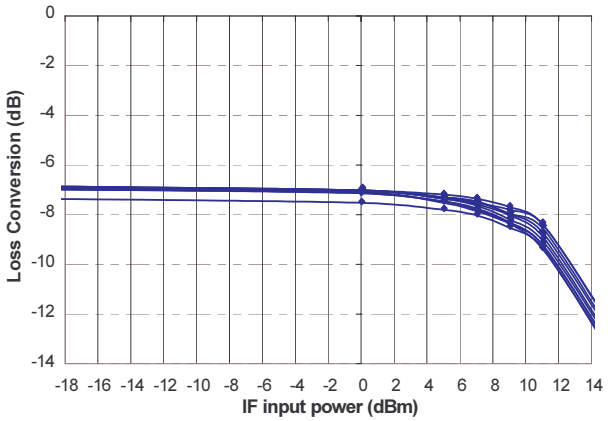

Fig. 8. Conversion loss as a function of IF input power, P_{LO}=10 dBm, F_{IF}=7 GHz, F_{LO}=5.7 GHz.

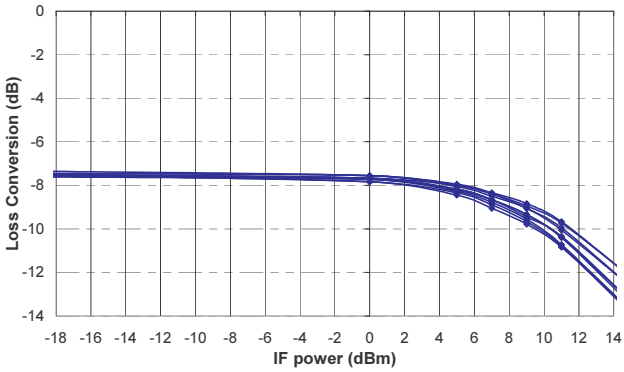

Fig. 9. Conversion loss as a function of IF input power, P_{LO}=10 dBm, F_{IF}=7 GHz, F_{LO}=3 GHz.

CONCLUSION

For use as up-converter in cost effective Ka-band VSAT outdoor units, the design and performance of an highly integrated mixer with a double input for balanced operation has been presented. While only occupying a GaAs area of 2.9 mm2, the 30 GHz mixer exhibits broadband performance, with up-converter loss of only 8 dB and up to 10-GHz IF frequency. By replacing up to five MMICs, this compact self-bias up-converter IC represents a reduction by at least a factor of three in the amount of GaAs area required to achieve the same functions, and allows significant reduction in module complexity, assembly, and filtering.

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