A balanced InGaP-GaAs Colpitt-VCO MMIC with ultra-low phase noise

Herbert Zirath*#, Rumen Kozhuharov*, Mattias Ferndahl*

*Chalmers University of Technology, Microwave Electronics Laboratory, MC2, SE-412 96, Göteborg, Sweden
Ericsson AB, Microwave and High Speed Electronics Research Centre, Mölndal, Sweden.

ABSTRACT — A balanced VCO-MMIC based on a coupled Colpitt topology with a fully integrated tank is presented. The design was focused on achieving minimum phase noise by optimization of the tank-circuit including the varactor, maximizing the tank-amplitude, and designing the VCO for Class C operation. A minimum phase noise of less than -112 dBc at an output power of 5.5 dBm is achieved at 100 kHz carrier offset and 6.4 GHz oscillation frequency. To our best knowledge, this is the lowest reported phase noise to date for a varactor based VCO with a fully integrated tank. The MMIC was designed and fabricated in a commercial InGaP-GaAs HBT foundry MMIC-process.

I. Introduction

In modern wireless communication systems, for more advanced digital modulation schemes, a phase noise as low as -110dBc@100kHz frequency offset might be demanded. Such low phase noise can utilized by using a dielectric stabilized oscillator, but is difficult to realize with MMIC-based VCOs with on chip varactor at microwave frequencies. The HBT technology is regarded to be the best-suited technology choice for VCOs due to a low 1/f noise. The status of MMIC-based VCOs obtained from the literature is presented in Fig. 1. The obtained phase noise as a function of frequency at an offset frequency of 100 kHz is plotted along with 20dB/decade slope-lines. Line 1 represents results using a PHEMT based reflection topology, line 2 represents the best III-V HBT VCOs, Si-CMOS and a few MESFET and HEMT based VCOs. SiGe HBT VCOs have shown impressive performance. The ref. [24] in Fig 1 is a SiGe-HBT MMIC oscillator based on a balanced Colpitt design serving as a pre-study to this work showing that very low phase noise can be obtained with this oscillator topology. Although this design has no varactor, the tank circuit is completely integrated. For even lower phase noise, combining methods can be considered. This was demonstrated on an SiGe HBT technology by Jacobsson et al. [1] showing that phase noise can be improved 1-3 dB, and 3-6 dB for double and quadruple VCO-design respectively. An InGaP/GaAs HBT of common emitter reflection type [2], represented by [27] in Fig.1, has shown similar phase noise levels but this design has very limited tunability, only 12 MHz. Line 3 represents state-of-the-art in phase noise of MMIC oscillators with integrated tank. The result presented in this work is also plotted in the diagram.

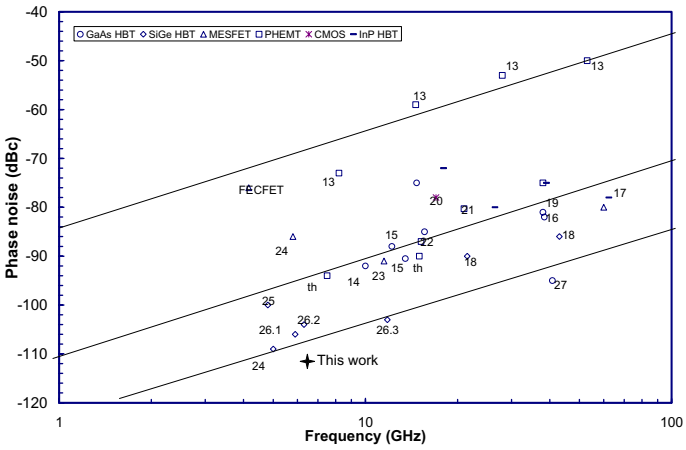

Fig 1 Phase noise plot of reported MMIC VCOs.

II. Choice of VCO topology and design strategies

In this work, an InGaP-HBT, varactor tuned, coupled Colpitt VCO design based on a commercial foundry (Knowledge*on) is implemented. The schematic of the VCO is shown in Fig 2 (simplified bias network).

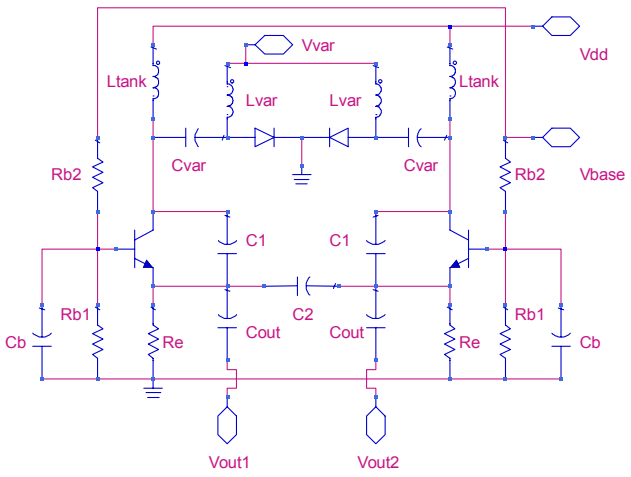

Fig 2 Schematic of the the InGaP-GaAs HBT VCO

The reason for choosing the Colpitt oscillator topology is its favorable impulse sensitivity characteristics as described by Lee and Hajimiri [3], which is the key for

achieving low phase noise. The popular 'negative gm' topology [4], used widely in balanced designs has the advantage of generating a negative resistance over a larger frequency range while the Colpitt oscillator's negative resistance is restricted in frequency by it's external feedback elements according to [4]

$$R = -\frac{g_m}{C_1 \cdot C_2 \cdot \omega^2}$$

The Colpitt oscillator can however be designed to operate in a more nonlinear mode where the current to the tank-circuit is delivered in narrow pulses thus minimizing the impulse sensitivity. It is therefore important that the transistor can deliver a high peak current during the duration of the pulse. This is one advantage of the HBT compared to a FET/HEMT.

In this design, a VCO-topology based on two separate grounded gate Colpitt VCOs that are tightly coupled, is studied. The arrangement with two coupled oscillators gives a 3 dB improvement in phase noise compared to a single oscillator [5]. The balanced Colpitt VCO topology was first successfully implemented in a PHEMT-technology with dramatic improvement in phase noise compared to various 'negative resistance' VCO designs based on the same PHEMT-technology [6].

Instead of using two separate feedback grounding capacitors to the emitter (one for each oscillator), one single capacitor is 'cross connected' between the emitters. Since the oscillators are oscillating out of phase, a virtual ground is formed inside this capacitor. This topology has the advantage saving one capacitor, in addition no RF-ground currents have to circulate, and the size of the capacitor is reduced by a factor of two.

Other criteria for achieving low phase noise are given by Leeson's formula for phase noise:

$$L(\Delta\omega) = 10 \cdot \log\left\{\frac{2 \cdot F \cdot k \cdot T}{Psig}\left[1+\left(\frac{\omega_0}{2 \cdot Q \cdot \Delta\omega}\right)^2\right] \cdot \left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right\}$$

F represents the noise figure of the transistor, T is the temperature, k is Boltzmann's constant, P_{sig} is the signal power, Q is the loaded Q-value of the tank, ω_0 is the oscillation frequency, $\Delta\omega$ is the offset from the oscillation frequency, $\Delta\omega_{1/f}^2$ is the corner frequency for 1/f noise. The equation is phenomenological and useful in order to get an understanding how phase noise should be minimized. In general, the Q-value of the tank should be maximized, the oscillation amplitude in the tank should be maximized, and the noise generated by the transistor should be as small as possible. All these criteria were taken into account when designing this VCO. Special emphasis was given to the varactor design in order to achieve a high Q-value. The varactor was realized utilizing the B-C junction layers in the epistack, and optimizing the layout for a minimum series resistance.

III. Simulation procedure and results

The design was made sequentially/iteratively according to following procedure:

1. Loop gain analysis

A small signal analysis of the loop gain is performed assuring that the loop gain is larger than 1 for frequencies of interest.

2. Waveform optimization

A harmonic balance simulation is performed where the collector current and collector-emitter voltage waveforms are adjusted for minimum conduction angle, the tank voltage should have a magnitude comparable with the breakdown voltage of the HBT. If the tank voltage is too small, the transistor area has to be increased and the design has to start from step1. V_{CE} of the HBT is monitored, and the HBT should not be allowed to reach into the saturation region.

3. Varactor voltage sweep

The phase noise is checked over the varactor voltage range. Any abnormal increase in the phase noise can normally be tracked down to the I_C-V_{CE} waveform performed in step 2

4. Layout generation

The layout is done in this step, during the layout work, harmonic balance simulations are performed ensuring that the waveforms don't change.

5. Redesign after layout

Due to the parasitic elements introduced by the layout, the design has to start from step 2 again if an increase in phase noise is introduced by the layout step.

In the final design, HBTs of emitter size 4x2x20 is used. This size gave the best overall performance. ADS2003A from Agilent was used for the simulation and layout of this VCO. Some simulation results are shown below; the DC and RF collector current amplitudes are plotted in Fig. 3, the I_C-V_{CE} trajectory together with the static I_C-V_{CE}-characteristic in Fig. 4, the phase noise @100kHz in Fig. 5, and the tank-inductor current/tank-voltage amplitudes in Fig. 6. Vbias is the independent variable in the simulations, Vbias controls the DC-current of the HBT and therefore also the RF-amplitude in the tank. The collector supply voltage is set to 5V. The predicted oscillation frequency is 6.9 GHz.

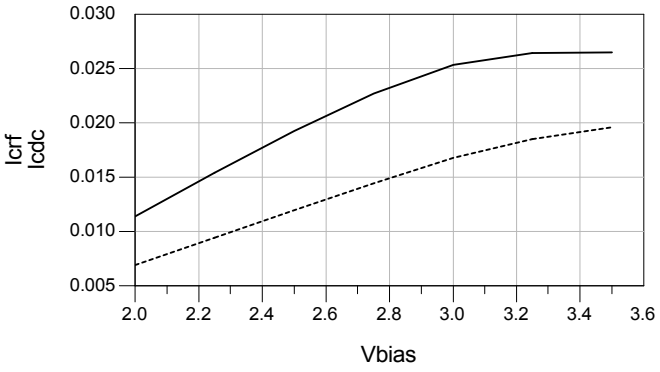

Fig. 3 Amplitude of the RF- (full line) and DC-collector current (dashed) versus Vbias.

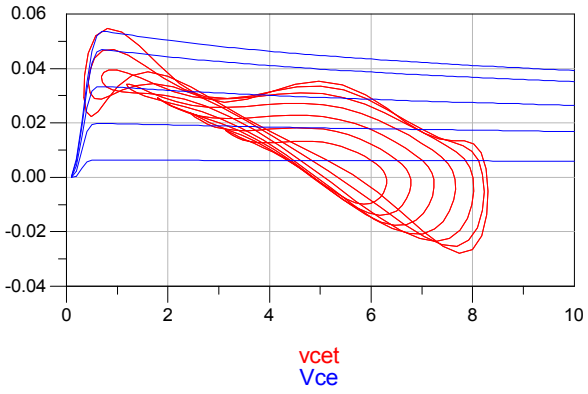

Fig. 4 I_C-V_{CE} trajectory for different base bias, Vbias, for one HBT in the VCO together with the static I_C-V_{CE} characteristic. The collector supply voltage is 5 V.

For the static I_C-V_{CE}-characteristic, the base current varies from 50 µA to 450 µA with 100 µA steps. The trajectories correspond to a Vbias from 2 to 3.5 V with a step of 0.25 V. As can be seen from Fig. 4, The collector current follows the static Ic-V_{CE}-characteristic in the saturation region. This occurs at a Vbias of approximately 3V. In this mode of operation, the phase noise is increasing as can be seen from Fig. 5.

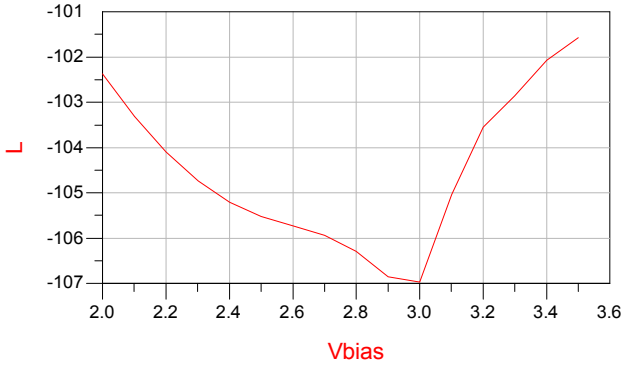

Fig. 5. The simulated phase noise at an offset frequency of 100kHz

From Fig. 3-5 we get the knowledge that the collector amplitude and the operation of the VCO can be effectively controlled by the dc base-current and that there is a clear minimum in the phase noise, which is related to the maximum tank amplitude just before the onset of transistor saturation. The peak collector current for this case is approximately 40 mA and the corresponding DC-collector current is 17 mA. The tank voltage amplitude and current through the tank inductor is plotted in Fig. 6. The tank amplitude at the onset of saturation is 8V and the corresponding inductor tank current is 210 mA !

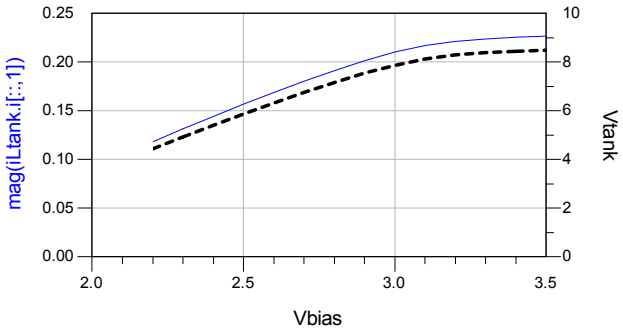

Fig. 6 The amplitude of the tank inductor current and the tank voltage (dashed line) versus Vbias.

A photograph of the VCO is shown in Fig. 3.

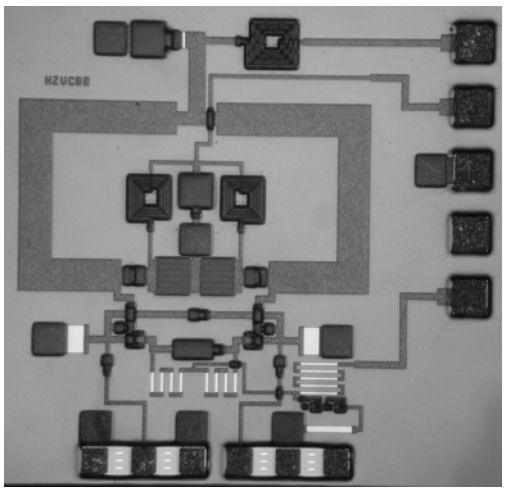

Fig. 7 Photograph of the InGaP-GaAs HBT VCO.

The circuit area is 1.5x1.6 mm^2. The outputs are balanced; CPW-pads for the outputs are located at the bottom of the chip. The supply voltage, varactor control voltage, and base bias are connected at the right side of the chip. It is possible to adjust the base voltage externally for any adjustment of the core current; this will control the output power and phase noise. The design was implemented in a commercial InGaP-GaAs HBT process named HS offered by Knowledge*on [6]. The

HBTs in this process has an f_T and f_{max} of >60 GHz and >110 GHz respectively, a breakdown voltage BV_{CE0} of >10V, and a DC gain of 130.

IV. Measurement Results

The oscillation frequency versus varactor voltage and output power versus varactor voltage is plotted in Fig. 8 and Fig. 9. The measured frequency is approximately 500 MHz above the predicted. The signals from the two output ports were combined in an external 180 deg hybrid. The measured output power corresponds well with the simulated value of 5.5 dBm and varies only slightly with the varactor voltage.

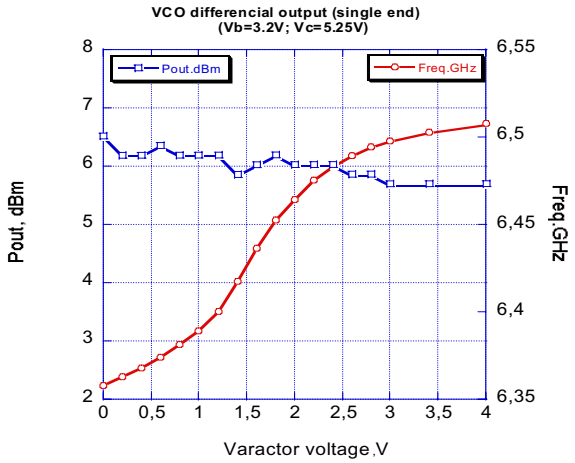

Fig 8 Output power and frequency versus varactor voltage

The phase noise was measured both with a spectrum analyzer, and with an Agilent E5500 phase noise system 'on wafer' in a shielded probe station. A minimum phase noise of less than –112 dBc is obtained at an offset frequency of 100kHz at 6.4 GHz, and an output power of 5.5 dB_m. The measured phase noise is 4-5 dB lower compared to the simulation. The current consumption of the VCO is 33 mA at Vbias=3V.

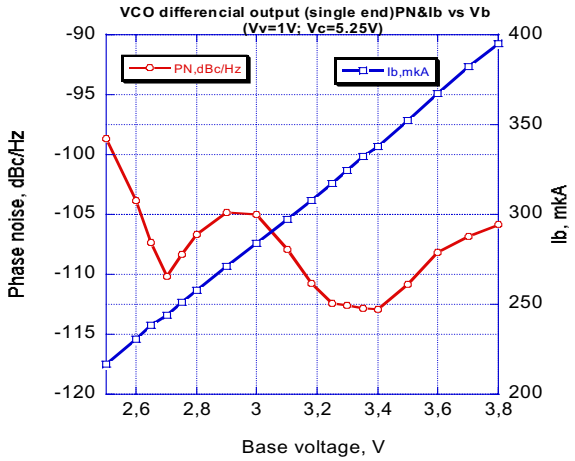

Fig 9 Phase noise and core current versus base bias voltage

This corresponds well with the simulation which predicts 34 mA. The predicted minimum of the phase noise as a function of bias voltage is also predicted but there is an additional minimum in the phase noise which was not predicted by the simulation.

This output power is comparatively high compared to other designs based on for instance SiGe HBTs, with very little variation of the power as a function of varactor voltage. To the knowledge of the authors, the phase noise result represents state-of-the-art for *any* VCOs with on-chip tuning varactor. The oscillator shows a 30 dB/decade slope between LF and 100kHz, above 100kHz the slope is 20dB/decade.

V. Summary and Conclusions

An InGaP-GaAs HBT based VCO based on a coupled Colpitt topology with an integrated tank including an optimized varactor was simulated, fabricated, and characterized. The VCO was optimized for low phase noise considering the tank Q-value, impulse sensitivity, oscillator amplitude (and the ability to control it), and transistor size. The measured phase noise is less than -112 dBc@100kHz at an oscillator frequency of 6.4 GHz. To our best knowledge, this represents state-of-the-art for a VCO with a fully integrated tank described in the research literature.

Acknowledgement

The Swedish Foundation for Strategic Research, SSF, the Swedish Agency for Innovation Systems, VINNOVA, Chalmers Center for High Speed Technology, CHACH are acknowledged for financial support. The interest from Sven-Ingmar Ragnarsson, Per Ericsson, Jan Grahn, Anders Sjölund, Arne Alping, Thomas Lewin, Jonas Noreus, Mikael Öhberg is highly appreciated. Agilent is acknowledged for donation of the ADS software.

References

[1] H. Jacobsson, B. Hansson, H. Berg, S. Gevorgian,'Very Low Phase-Noise Fully-Integrated Coupled VCOs', 2002 Radio Frequency Integrated Circuits Symposium, paper IF-TU-52, pp. 467-470, 2002.

[2] M.S. Heins, D.W. Barlage, M.T. Fresina, D.A. Ahmari, Q.J. Hartmann, G.E. Stillman, M. Feng,'Low Phase Noise Ka-band VCOs using InGaP/GaAs HBTs and Coplanar Waveguide', 1997 IEEE MTT-Digest, pp.255-258, 1997.

[3] A. Hajimiri, T Lee,'Low Noise Oscillators', ISBN 0-7923-8455-5, Kluwer Academic Publishers, 1999.

[4] B. Razavi,'Design of Analog CMOS Integrated Circuits', ISBN 0-07-118815-0, McGraw-Hill, p. 508-509, 2001.

[5] B. Razavi,'RF Microelectronics', ISBN 0-13-887571-5, Prentice Hill PTR, p. 224, 1998.

[6] H. Zirath, T. Masuda, R. Kozhuharov, M. Ferndahl,'Development of 60 GHz front end circuits for high data-rate communication systems', Accepted for publication in IEEE J. Solid State Circuits.

[6] www.knowledge-on.com