Faster and Smaller with Carbon Nanotubes?

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***Abstract* — Carbon Nanotubes seem to be one of the most promising candidates for nanoelectronic devices beyond presumable scaling limits of silicon and compound semiconductors and independent from lithographic limitations. Discovered only about a decade ago, there has been a tremendous advance in the field of carbon nanotubes. Their exciting properties, especially with respect to electronic applications, and their fabrication methods will be discussed. A variety of Carbon Nanotube based electronic devices, such as interconnects, transistors, and power transistors, will be presented. However, large-scale integration of carbon nanotubes seems to be a huge challenge. Some of the integration issues will be critically addressed and carbon nanotubes will be compared with some other nanoscale approaches.**

I. Introduction

An increasing number of technological and physical problems will evolve in the next decade if the scaling of integrated circuits (ICs) continues. This fact is clearly emphasized in the international roadmap of semiconductors (ITRS), a guideline for microelectronic manufacturing [1]. The ITRS clearly indicates that an increasing number of technological challenges will evolve in the next couple of years. The rather constant shrinking of feature sizes observed over the last three and a half decades is called Moore's law. It says that roughly every 18 month the component count is doubling, leading to an exponential growth in the complexity of IC chips. If this trend continues one eventually needs a semiconducting material with a higher mobility and a higher current density to replace silicon in field effect transistors (FETs). The situation will also get critical for interconnect materials since electromigration and the size effect will pose a physical limit to the scaling of metal interconnects. Electromigration appears at high current densities and will cause interconnect failure by formation of voids. This effect will become more and more pronounced if the current densities have to increase due to continuous shrinking of the cross-section of interconnects. The size effect is related to surface and grain-boundary scattering, which will considerably gain influence in smaller interconnects. Therefore, new materials have to be considered. Carbon nanotubes (CNTs) and nanowires seem to be promising candidates that might eventually replace some of the materials used in today's microelectronic manufacturing.

Besides of those physical constraints there might also be a limit for today's top-down approaches in which structures of an IC are obtained by subtractive patterning (lithography and etching processes). In contrast to top-down processes bottom-up approaches are able to yield nanometer scale structures by self-assembly. Examples are the catalytic synthesis of carbon nanotubes or nanowires. Here nanometer sized catalyst particles act as the nucleation sites of the nanotubes or the single crystalline nanowires. The diameters of the nanotube or nanowires are defined by the diameter of the particle.

CNTs have been in the focus of research for some time since they have some exceptional electronic and mechanic properties and are an ideal example for self assembled one-dimensional (1-D) macromolecular systems. They can be thought of as a sheet of hexagonal ordered graphite (graphene) rolled-up to form a seamless cylinder (Fig. 1). They can be 0.4 – 30 nm in diameter with lengths up to millimeters. Several single-walled nanotubes (SWCNTs) can be concentrically nested inside each other forming a multi-walled carbon nanotube (MWCNTs).

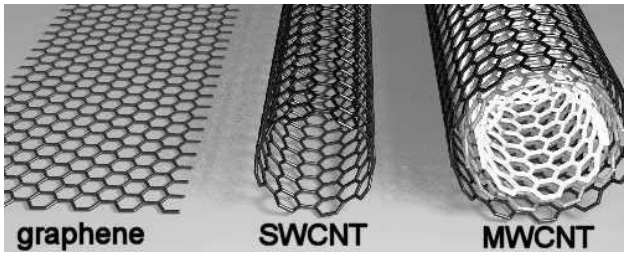

Fig. 1. "Evolution" of nanotubes from a two dimensional graphene sheet, over a SWCNT to a MWCNT consisting of several concentrically nested SWCNTs.

A nanotube can have different electronic properties depending on the way it is rolled up. This variety arises from the 2-dimensional structure of a single graphite sheet, which behaves like a zero bandgap semiconductor, and the 1-D structure of the nanotube confining the electrons in the circumferential direction. SWCNT can thus have either metallic or semiconducting properties. The bandgap of the semiconducting SWCNTs depends inversely on the diameter. Therefore large diameter SWCNTs and MWCNTs show a predominant metallic behavior. The electronic property of metallic SWCNTs with very small diameters is complicated by the large curvature of the rolled-up graphene sheet leading to the formation of a curvature induced bandgap.

A large number of possible applications have been proposed as a result of the variety of extraordinary properties exhibited by carbon nanotubes [2]. They can promote ballistic transport, allow very high current densities, and are less prone to interface states as compared to the silicon/SiO_2 interface. In particular, the high current carrying capacity and mechanical stability of

metallic nanotubes indicates applications in microelectronic interconnects [3] whereas the reasonably large band gap of SWCNTs with small diameters (< 3 nm) suggests their use as nanoscale transistors [4].

In the next chapter the fabrication of carbon nanotubes will be addressed. Then the potential of MWCNTs for interconnect applications will be discussed. The main focus will be on SWCNTs for transistors. Finally nanowires will be presented as a further example of self-assembled nanostructures.

II. CNT Synthesis

CNTs can be fabricated by three different methods: arc discharge evaporation, pulsed laser ablation (PLD), and catalytic chemical vapor deposition (CCVD) [5]. Arc discharge evaporation is based on evaporation of carbon in an arc between two graphite rods. In the direct arc the plasma reaches temperatures around 3000 °C. For the synthesis of MWCNTs no catalyst addition to the graphite rods is required, whereas SWCNTs synthesis is only possible if small amounts of catalysts are added.

In a PLD processes a pulsed laser evaporates a target within a heated zone (~ 1200 °C) of a furnace. The target usually consists of graphite with small additions of catalyst metals (e.g. Co/Ni).

The nanotube material produced in arc discharge evaporation and PLD consists of a highly entangled "felt" of nanotubes, CNT bundles, amorphous carbon, and catalyst clusters. Therefore, this material first has to be cleaned, dispersed, cut, and finally deposited on a substrate. An oxidative process usually accomplishes cleaning. The dispersion is done by ultrasonication in appropriate solvents. Deposition on substrates can be done by spinning on, spraying on, or by adsorption. Unfortunately, the cleaning and ultrasonication might induce defects in the nanotube and thus deteriorate the electronic properties.

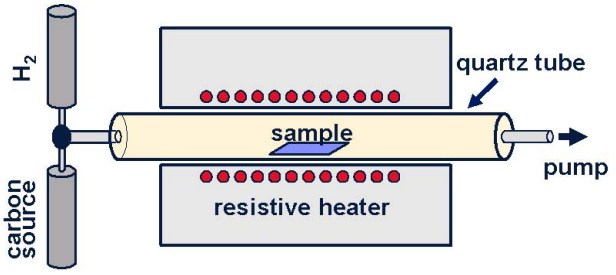

Fig. 2. Schematic of a CVD furnace as used for CNT growth.

The PLD and the arc-discharge process are based on the evaporation of carbon atoms at temperatures around 3000 °C, which are definitely incompatible with a substrate-based growth of CNTs. In contrast, CCVD has the inherent advantage that it allows direct and patterned growth of CNTs on a chip, and therefore does not require the laborious purification and dispersion treatment described above. Similar to arc discharge and PLD the CCVD synthesis of CNTs requires catalyst clusters that act as nucleation sites for the CNTs. CCVD growth of CNTs is usually performed at temperatures between 600°C and 1000 °C and by using an appropriate carbon containing feedstock gas (Fig. 2).

SWCNTs and MWCNTs can be grown by CCVD in about the same temperature range. Basically, the size of the catalyst particle will determine whether a SWCNT or a MWCNT can nucleate. Small catalyst clusters < 3 nm favor the growth of SWCNTs. For good growth a variety of parameters have to be considered such as catalyst layer thickness, catalyst support, carbon precursor, pressure, temperature, or pretreatment time.

CCVD is the widely preferred method for integration of CNTs because of the advantages mentioned above.

III. MWCNTs For Interconnects

Nowadays chips have become almost "all wire". The transistors at the bottom make up only a fraction of the total chip, and already today, the speed and performance of such chips is mainly limited by the interconnects, i.e. the copper-based wiring of the transistors with different metal layers (wires) and the vertical connections between these layers, which are called vias. These vias are prone to electromigration failures. In 2013 the ITRS [1] predicts a current density of 3.3 10^6 A/cm^2 in a via. Such values can to date only be supported by CNTs, where current densities exceeding 10^9 A/cm^2 have been reported. At this ITRS technology node a MPU/ASIC half-pitch of 32 nm is predicted. On this scale, traditional interconnect schemes become problematic due to the increasing wire resistances resulting from grain and surface scattering effects and the higher current densities which must be carried [6]. Sufficient heat removal from the chip is already a problem in nowadays computers. Nanotubes may also help to remove the heat more efficiently from the chip due to their superb thermal conductivity, which exceeds that of diamond by a factor of two. Therefore, CNTs would be ideal for vias and contact holes.

The main challenges for an integration of MWCNTs as interconnects are a required high structural perfection of the MWCNTs, precise control of the activity of individual catalyst particles, and low contact resistances. A high perfection is necessary to enable ballistic transport or at least a rather large mean free path. Unfortunately, ballistic transport has only been observed on MWCNTs grown by catalyst free arc-discharge evaporation up to now [7]. Control of the catalyst activity is necessary to obtain a sufficient yield. Finally, MWCNTs will only have a chance to beat conventional metallization schemes if the contact resistances are sufficiently small.

Recently, we demonstrated the first steps on the way to MWCNTs as vertical interconnects by achieving the growth of individual MWCNTs from the bottom of lithographically defined holes with 20-60 nm diameters (Fig. 3.). Vertical interconnects could be realized by using a Ta/Fe catalyst multilayer at the bottom and a Ti top contact. Nevertheless, the bottom contact is still a critical issue that has to be substantially improved.

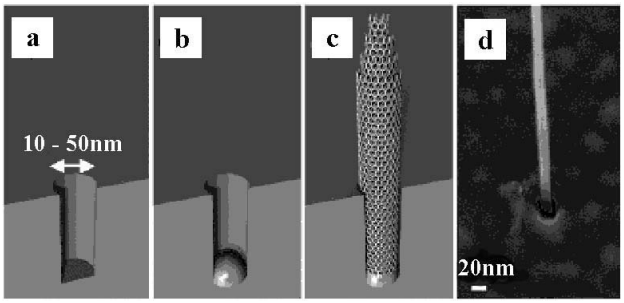

Fig. 3. a) - c) In a 10- 50 nm wide nano-hole a catalyst is deposited and MWCNTs are grown. d) SEM micrograph of a single MWCNT of 20 nm diameter protruding from a nano-via.

The MWCNT growth is usually carried out at temperatures between 600 °C and 700 °C. Those temperatures are still too high to be competitive with standard MOSFET backend processes. To reduce the growth temperature one can enhance the growth by a plasma (microwave plasma, inductively coupled plasma…) [8]. Unfortunately, the detrimental effect of plasma processes is often the increased defect density due to the presence of high energetic particles.

IV. SWCNT Field Effect Transistors

The largest challenges for the integration of SWCNTs nanotubes arise from the fact that until now only mixtures of SWCNTs with metallic and semiconducting SWCNTs can be produced. A separation or selective modification according to their electronic properties seems to be a prerequisite for a successful integration into electronic devices. Recently, some separation methods have been suggested. However, they still lack in precision, yield, and in some cases still require proof by electronic characterization of the separated material [9-11]. Hence, preferential breakdown is still the only straightforward method to eliminate the metallic tubes. Preferential breakdown can be achieved by depleting the semiconducting SWCNTs with an appropriate gate voltage and then applying a high bias to burn the metallic SWCNTs [12]. Further, the precise placement of SWCNTs is still in their infancy. Placement of SWCNTs on a substrate can either be achieved by deposition from solutions (e.g. spin-on, adsorption…) or by CCVD growth from predefined catalyst islands. The precision of both approaches is still very insufficient.

Using the latter approach, we could obtain SWCNTs that are in-situ contacted. The SWCNTs were grown by CCVD between lithographically defined electrode structures. The direct growth on metal electrodes is possible by introducing a thin Al_2O_3 separation layer. The in-situ formed contacts still have very high resistances. By using electroless Ni- or Pd-deposition we could considerably improve the contacts. The electroless deposition is a self-aligned process, which does not require an additional lithography. Similar self-aligned processes will be the key to future nanoelectronic devices.

The first SWCNT FETs did use the silicon substrate as the backgate. For an IC it is however essential that the transistors can be individually addressed. This can be accomplished by e.g. depositing a gate dielectric and a gate electrode between source and drain contacts on top of the nanotube. Such topgates were presented by a number of groups. By depositing thin layers of high-k dielectrics subthreshold slopes of up to 80 mV/decade have been reported [13]. We succeeded in the fabrication of topgates using a very simple dip coat process to deposit a 5-10 nm thick Ta-oxide layer (Fig. 4a). The subthreshold slopes of those devices are usually around 150 mV/decade.

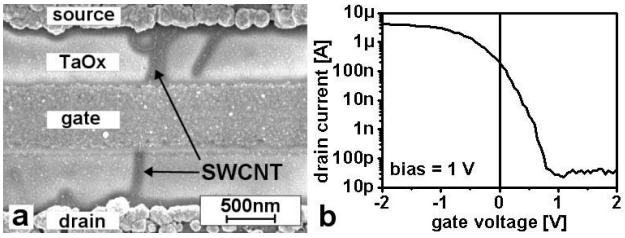

Fig. 4. a) A top gated SWCNT with a 5 nm Ta-oxide layer as gate dielectric and a thin Al layer as the gate electrode. The source and drain contacts were improved by electroless Pd-deposition. b) Drain current vs. gate voltage curve of a SWCNT with a topgate measured at a bias of 1 V.

As can be seen in Fig. 4b, semiconducting SWCNTs show usually p-type characteristics, which has been attributed to doping by adsorbed oxygen. The p-type SWCNT can be transformed into n-type SWCNTs by annealing in vacuum or alkali metal doping. That way it was possible to demonstrate logic gates by linking a small number of SWCNT-FETs [14,15].

The initial studies of SWCNTs were mainly focusing on FETs with individual nanotubes. Single nanotube transistors can usually switch currents of less than 20 µA. For applications that require higher currents one needs several SWCNTs in parallel. Recently we have demonstrated that planar FET consisting of a large number of parallel SWCNTs allow very high on-currents of the order of milliamperes and on/off ratios exceeding 500 (Fig. 5a).

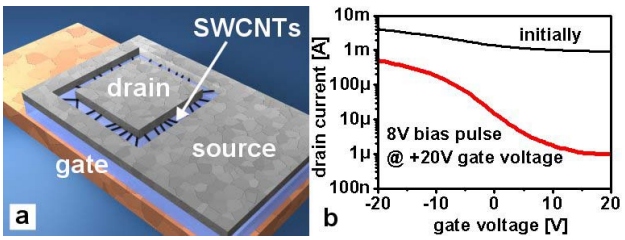

Fig. 5. a) Schematic of a high current SWCNT transistors consisting of randomly grown SWCNTs. b) Drain current vs. gate voltage curve of such a transistor before and after elimination of most of the SWCNTs with some metallic conductance by a bias pulse and the gate voltage at +20V.

With these devices it was demonstrated, for the first time, that SWCNTs can be used as transistors to control macroscopic devices. Those transistors were fabricated by a simple process that is based on the random CCVD growth of SWCNTs at low temperatures, a single lithographic step to define the source and drain contacts

(Pd-electrodes), and a bias pulse to eliminate the SWCNTs with metallic contribution (Fig. 5b). Of course the performance of those high-current transistors is by far not yet optimized. Key to an improved performance is a selective growth of exclusively semiconducting SWCNTs or a reliable separation of the semiconducting SWCNTs from metallic SWCNTs and SWCNTs with a small bandgap.

Besides understanding the principal electronic transport characteristics of CNTs it is of course also important to asses their operation at high frequencies. The first studies of the RF properties of carbon nanotubes have been performed just very recently. So, operation of SWCNT transistors at microwave frequencies (2.6 GHz) and operation of a MWCNT rf-single electron transistor have been claimed [16,17]. The ballistic transport observed in rather short semiconducting SWCNTs (< 300 nm) and the reported mobilities of as much as 10000 cm^2/Vs will hopefully favor high frequency applications.

V. Nanowires

Nanowires might be an alternative to carbon nanotubes. They are also 1-D devices but do not have a hollow structure. The main advantage of nanowires is the better control of their electronic properties. One does not obtain the mixture of various electronic properties as in the case of SWCNTs and the electron and hole doping can already be controlled during synthesis. However, their disadvantage is that they do not promote ballistic transport and are prone to the same problems known from today's semiconductor devices (e.g. low maximum current densities, high power dissipation, interface states, surface scattering).

Nanowires have been synthesized by a variety of processes, e.g. laser ablation [18,19], solvothermal growth under high pressures [19], and CCVD [20-22]. CCVD of nanowires offers again the advantage of patterned growth. Si and Ge nanowires have been successfully fabricated by CCVD. Temperatures during CCVD of nanowires can be as low as 275 °C [22], which is substantially lower than the minimum growth temperatures of nanotubes (600 °C). Some rather high mobilities have been reported for nanowire FETs, e.g. nanowire FETs build of 10-20 nm diameter Si nanowires or 20 nm Ge nanowires exhibited mobilities of up to 1000 cm^2/Vs and 600 cm^2/Vs, respectively [23,24].

VI. Conclusion

Carbon nanotubes have very exceptional electronic properties. However, integration into electronic devices will only be successful if precise control of their structure, their contacts, and their location can be achieved. Prototypes of SWCNT transistors did already demonstrate a performance compatible with high-end MOSFET transistors and showed superior current densities. Besides of the large hype of the nanotube topic one has to bear in mind that it will take enormous research efforts before nanotubes can compete with conventional concepts used in today's microelectronic manufacturing. Nanowires are another example for self-assembled nanostructures. Yet is has to be shown whether they are superior to conventionally patterned semiconductors with similar dimensions.

Acknowledgement

We thank Dr. W. Pamler for the artwork. This work was supported by the German Ministry of Science and Technology (BMBF) under Contract No. 13N8402.

References

[1] International Technology Roadmap for Semiconductors: http://public.itrs.net/Files/2003ITRS/Home2003.htm
[2] P. G. Collins and Ph. Avouris, Nanotubes for Electronics, *Scientific American*, Dec. 2000, 38.
[3] F. Kreupl, A. P. Graham, G. S. Duesberg, W. Steinhoegl, M. Liebau, E. Unger, and W. Hoenlein *Microelectronic Engineering*, 64, 2002, 399.
[4] Phaedon Avouris, Molecular Electronics with Carbon Nanotubes, *Acc. Chem. Res.*, 2002, 35, 1026.
[5] R. Saito, G. Dresselhaus, and M. S. Dresselhaus, "Physical Properties of Carbon Nanotubes" *Imperial College Press*, 1998.
[6] W. Steinhoegl, G. Schindler, G. Steinlesberger, and M. Engelhardt, *Phys. Rev. B*, 2002, 66, 75414.
[7] P. Poncharal, C. Berger, Y. Yi, Z. L. Wang, and W. A. de Heer, *J. Phys. Chem. B. (Review)*, 2002, 106, 12104.
[8] M. Meyyappan, L. Delzeit, A. Cassell, and D. Hash, *Plasma Sources Sci. Technol.*, 2003, 12, 205.
[9] R. Krupke, F. Hennrich, H. v. Lohneysen, M. M. Kappes, *Science*, 2003, 301, 344.
[10] M. Zheng, A. Jagota, M. S. Strano, A. P. Santos, P. Barone, S. G. Chou, B. A. Diner, M. S. Dresselhaus, R. S. McLean, G. B. Onoa, G. G. Samsonidze, E. D. Semke, M. Usrey, and D. J. Walls, *Science*, 2003, 302, 1545.
[11] Z. Chen, X. Du, M.-H. Du, C. D. Rancken, H.-P. Cheng, and A. G. Rinzler, *Nano Lett.*, 2003, 3, 1245.
[12] P. G. Collins. M. S. Arnold, and Ph. Avouris, *Science*, 2001, 292, 706.
[13] A. Javey, J. Guo, D. B. Farmer, Q. Wang, D. Wang, R. G. Gordon, M. Lundstrom, and H. Dai, *Nano Lett.* 2004, 4, 447.
[14] A. Bachtold, P. Hadley, T. Nakanishi, and C. Dekker, *Science*, 2001, 294, 1317.
[15] V. Derycke, R. Martel, J. Appenzeller, and Ph. Avouris, *Nano Lett.*, 2001, 1, 453.
[16] Li, S.; Zhen, Y.; Yen, S.-F.; Tang, . C., Burke, P. J. *Nano Lett.* 2004, 4, 753.
[17] Roschier, L.; Hakonen, H.; Bladh, K.; Delsing, P.; Lehnert, K. W.; Spietz, L.; Schoelkopf, R. J. *J. Appl. Phys.* 2004, 95, 1274
[18] A. Morales and C. M. Lieber, *Science*, 1998, 279, 208.
[19] P. Yang, Y. Wu, and R. Fan, *Int. J. Nanosci.*, 2002, 1. 1.
[20] J.-Y. Yu, S.-W. Chung, and J. R. Heath, *J. Phys. Chem. B*, 2000, 104, 11864.
[21] Y. Cui, L. J. Lauhon, M. S. Gudiksen, J. F. Wang, and C. M. Lieber, *Appl. Phys. Lett.*, 2001, 78, 2214.
[22] D. Wang and H. Dai, *Angew. Chem.*, 2002, 41, 4783.
[23]Y. Cui, Z. Zhong, D. Wang, W. U. Wang, and C. M. Lieber, *Nano Lett.*, 2003.
[24] D. Wang, Q. Wang, A. Javey, R. Tu, H. Dai, H. Kim, P. C. McIntyre, T. Krishnamohan, and K. C. Saraswat, *Appl. Phys. Lett.*, 2003, 83, 2432.