

Low Noise and High Linearity LNA based on InGaP/GaAs HBT for 5.3 GHz WLAN

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Abstract — This paper presents a low noise and high linearity LNA based on InGaP/GaAs HBT for 5.3 GHz WLAN. Previous LNAs based on FET series such as HEMT show excellent noise characteristics, but poor linearity. The InGaP/GaAs HBT LNA shows excellent linearity and noise characteristics because of its high base doping concentration. The proposed LNA is fully integrated in area of 0.9×0.9 mm² single chip with high Q spiral inductors and MIM capacitors and biased at current point for optimum noise figure and gain characteristics, furthermore, excellent linearity is achieved. Measured result of the proposed LNA shows 13 dB gain, 2.1 dB noise figure, and excellent linearity in terms of IIP3 of 5.5 dBm. The figure of merit (FOM) defined as a function of the linearity and noise figure is 20.1 dB, which is the best result among previous LNAs.

I. INTRODUCTION

This paper presents a low noise and high linearity LNA based on the InGaP/GaAs HBT, which has been used for mainly high power amplifier design, for 5.3 GHz WLAN band applications. The LNA is a very important device which is placed in front of receiver and determines noise figure of the whole receiver. Main performance parameters of the LNA are the gain, noise figure, and linearity. Among them, the gain and noise figure directly affect the noise figure of the whole receiver and the previous researches of the LNA are focused on the gain and noise figure. But, the LNA is connected with the power amplifier of the transmitter by a duplexer, and output power leakage degrades whole receiver sensitivity by saturation and the inter-modulation. So, the linearity of LNA is a very important performance parameter, but LNAs based on FET series such as HEMT and CMOS show excellent noise figure but poor linearity because of low Early voltage and etc of FET. This paper proposes a high performance LNA which shows excellent not only noise figure but also linearity. The InGaP/GaAs HBT shows high linearity and high frequency performance, and it is preferred for the design of power amplifiers. Moreover, InGaP/GaAs HBT base is highly doped for high linearity and high operating frequency. In result, the base resistance of InGaP/GaAs HBT is very small, and InGaP/GaAs HBT shows low noise figure [1]. For this reason, the InGaP/GaAs HBT can be suitable device for not power amplifier but LNA. The proposed LNA is designed and fabricated in 5.3 GHz WLAN band, and integrated in single chip with active, passive components, and pads for bias and signal input output.

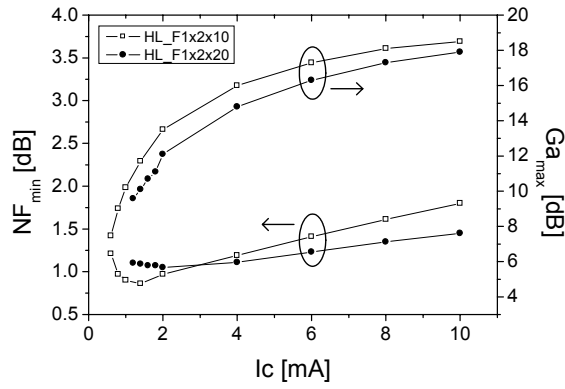
II. DESIGN AND IMPLEMENTATION

This paper presents a low noise figure and high linearity LNA based on InGaP/GaAs HBT for 5.3 GHz WLAN which is rise commercial value in nowadays. The device used for design is 2 μ m emitter length InGaP/GaAs HBT process. The InGaP/GaAs HBTs considered for design are HL_F1 \times 2 \times 10 and HL_F1 \times 2 \times 20, which have one finger and 10 μ m emitter width and 20 μ m, respectively. Those devices show excellent high frequency performance, 50 GHz unit current gain (f_T) and 80 GHz maximum oscillation frequency (f_{MAX}) at some bias conditions.

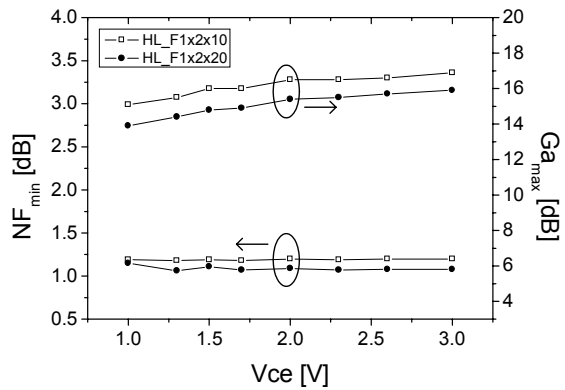
For the selection of the device, minimum noise figure (NF_{min}) and maximum available gain (MAG) are measured at various bias conditions. Fig. 1 is measured results of HL_F1 \times 2 \times 20 and HL_F1 \times 2 \times 10 at various collector currents and fixed collector-emitter voltage to 1.5 V. Fig. 1 (a) shows that HL_F1 \times 2 \times 20 has lower NF_{min} than HL_F1 \times 2 \times 10 over 2 mA collector current bias point. This is a result by that HL_F1 \times 2 \times 20 has roughly half base resistance than that of HL_F1 \times 2 \times 10. Also, MAGs are abruptly decreased less than 2 mA collector current points. This is resulted from that the device operation gets in to the cut-off region. Fig. 1 (b) is measurement results of MAG and NF_{min} of HL_F1 \times 2 \times 20 and HL_F1 \times 2 \times 10 at fixed collector current to 4 mA, and it shows that MAG is decreased and NF_{min} is increased with decrement of collector-emitter voltage, but it is not much influenceable. In other words, when the InGaP/GaAs HBT operates at forward-active region, MAG and NF_{min} are more sensitive function against collector current but collector-emitter voltage. Moreover, optimum bias points for MAG and NF_{min} is slightly different compared with FET series transistors. By above measurement result, the selected device for the LNA design is HL_F1 \times 2 \times 20 and 4 mA collector current bias point is selected for low noise figure and high linearity by stable forward-active region operation.

Fig. 2 is the equivalent circuit schematic of the designed LNA. The LNA topology is cascode amplifier and an inductor is inserted at emitter node on Q1. The cascode amplifier is stable by its high reverse isolation, and wide-band amplification and low noise can be achieved by cancellation of Mirror effect. Moreover, inductive de-generation using an inductor provides noise matching and gain matching at the same time, improved

III. EXPERIMENTAL RESULTS



(a)



(b)

Fig. 1. NF_{min} and MAG Characteristics with the Variation of (a) Collector Current and (b) Collector-Emitter Voltage.

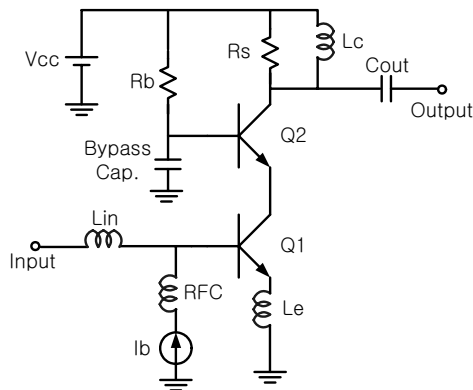


Fig. 2. Equivalent Circuit Schematic of the LNA based on InGaP/GaAs HBT.

linearity [2], and reduction of internal noise by feedback. Input and output matching of the presented LNA are implemented by on-chip passive devices. On-chip passive devices degrade noise characteristics of LNA by its high loss. Specially, the passive devices having low Q at input matching circuit is a main cause of degradation of the noise figure. For decreasing above effect, the capacitors are designed in form of high Q MIM capacitors, and the spiral inductors are fabricated with a thick metal layer, which is located above the insulator on substrate by posts, to achieve higher quality factor.

Fig. 3 is the photograph of the fabricated InGaP/GaAs HBT LNA, and chip size is $0.9 \times 0.9 \text{ mm}^2$. Measurement is performed on the Duroid ($\epsilon_r = 10$), which has very low high frequency loss, test board for accurate noise measurement. The fabricated chip is connected on the board by using silver paste and the input output signal line and bias line is connected by gold wire-bonding. For insulating external noise, conductor housing is used and isolates the chip and test board, and DC bias is applied by feed-through capacitors.

Fig. 4 is small signal measurement results. It is observed that 13 dB gain, -13 dB input return loss, and

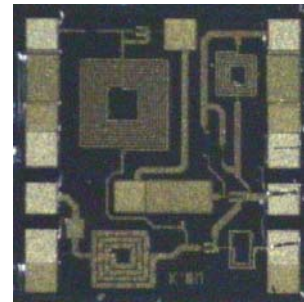
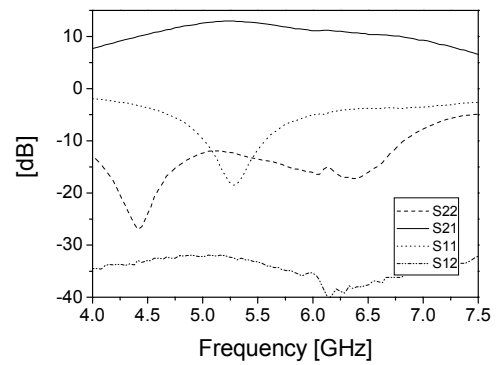
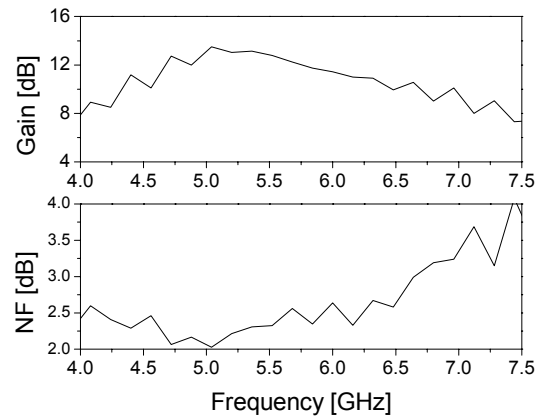


Fig. 3. Photograph of the fabricated MMIC LNA ($0.9 \times 0.9 \text{ mm}^2$).



(a)



(b)

Fig. 4. Small Signal Measurement Results (a) S-parameter (b) Noise Figure.

Reference	Freq. [GHz]	P_{dc} [mW]	Gain [dB]	NF [dB]	IIP3 [dBm]	FOM [dB]
CMOS [3]	5.7	14.4	12.5	3.7	-0.45	11.9
CMOS [4]	5.75	16.2	10.8	6.2	-6.5	1.2
SiGe BJT [5]	5.5	48	12	3.7	-2.3	3.4
SiGe BiCMOS [6]	5.5	26.4	18.7	4.2	-3.5	11.6
BiCMOS [7]	5	31	18.3	1.65	-3.95	11.7
MESFET [8]	5	13.2	11	1.9	5	16.9
HEMT [9]	2.4	21	12.5	1.6	-4.5	0.1
BiFET [10]	1.96	3.15	16	1.6	-6.5	8.7
GaAs HBT [11]	2	4	11.1	2.2	-0.1	8.8
HEMT [12]	2.4	1.7	15	1.8	-14	4.5
This work	5.3	12	13	2.1	5.5	20.1

TABLE I
PERFORMANCE COMPARISON WITH PREVIOUS LNAs

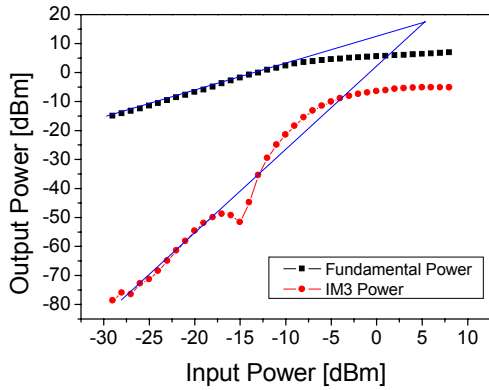


Fig. 5. Linearity Measurement Result.

-18 dB output return loss over the designed 5.3 GHz frequency range. The bandwidth defined by -10 dB input output return loss is 5.02 ~ 5.56 GHz, which satisfies WLAN band, the variation of gain over the entire bandwidth is 0.56 dB, and excellent reverse isolation, more than -30 dB, is observed in wide band. Measured noise figure of the fabricated LNA is 2.1 ~ 2.3 dB over the 5.02 ~ 5.56 GHz measured band. Fig. 5 is non-linearity measurement result. The fabricated InGaP/GaAs HBT shows excellent linearity in term of IIP3, 5.5 dBm.

For the estimation of performance of the fabricated InGaP/GaAs HBT LNA, various relevant LNAs based on CMOS, HBT, HEMT, BJT, and etc are compared. Previously published LNAs are summarized in Table I. According to Table I, the presented LNA shows excellent performance in aspects of noise figure and linearity compared with previous 5 GHz band LNAs ([3] - [8]). The presented LNA based on InGaP/GaAs HBT shows better or similar noise performance and superior linearity performance compared with LNAs base on FET series transistors. Moreover, compared with previous GaAs HBT LNA, the presented LNA shows superior noise and linearity characteristics [11]. The LNAs based on HEMT ([9], [12]) show good noise figure performance. However, the LNAs based on HEMT show but poor linearity compared with the presented InGaP/GaAs HBT LNA. The FOM (Figure of Merit) is calculated as a function of a noise figure (NF), IIP3, gain (G), dissipated power (P_{dc}), and operating frequency (f_0);

$$FOM [dB] = -NF$$

$$+ (IIP3 + G - 10 \log(\frac{P_{dc}}{1mW}) + 20 \log(\frac{f_0}{1GHz}))$$

(1)

The IIP3 added to the gain is the OIP3 which is generally proportional to the 1 dB saturation point and dissipated power. So, the IIP3 added to the gain is normalized to the dissipated power. Moreover, the gains of most of active devices are decreased by -20 dB/decade with respect to the increasing frequency. Therefore, the operating frequency normalized to 1 GHz is added to the FOM calculation. Consequently, the FOM indicates the generalized linearity and noise characteristics of the LNA. The calculated FOM of the fabricated LNA is 20.1 dB. It is the best measured FOM among previous LNAs. Precisely, for the design of high performance LNA, which satisfies low noise and high linearity, the InGaP/GaAs HBT can be an excellent device.

IV. CONCLUSION

This paper presents a low noise figure and high linearity 5.3 GHz band LNA based on the commercial InGaP/GaAs HBT process. For achieving superior gain and noise figure, the device, which has large base area, is selected and optimum collector bias point is selected by consideration of NF_{min} and MAG. Moreover, the high linearity is achieved from selection of large base area device. Inductor de-generation method is used for input matching and cascode topology contributes high gain and stability. The presented LNA shows 13 dB gain and 2.1 dB low noise figure in the measured band, 5.02 ~ 5.56 GHz, and shows excellent linearity in term of IIP3, 5.5 dBm. These results are excellent in aspect of noise figure and linearity compared with previous LNAs based on various devices. The fabricated LNA is fully integrated in area of $0.9 \times 0.9 \text{ mm}^2$ with passive, active devices and pads for input output signal and DC bias.

This paper presents high performance LNA based on InGaP/GaAs HBT, which has been used for mainly design of power amplifiers. From this research, this paper presents possibility about RF single chip design based on InGaP/GaAs HBT. Hereafter, if the research of RF single

chip design based on InGaP/GaAs HBT will be done, the InGaP/GaAs HBT can be an appropriate device for RF single chip design.

ACKNOWLEDGEMENT

This work has been supported by Basic Research Fund of Yonsei University. The authors would like to thank Knowledge*ON Semiconductor Inc. for the fabrication of the LNA circuit, using its 6 inch InGaP HBT foundry service and design library.

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