InP DHBT-Based IC Technology for High-Speed Data Communications

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***Abstract* — In this paper, we report the achieved performance of devices and integrated circuits (ICs) using a manufacturable InP DHBT-based technology. High speed MBE grown InGaAs/InP DHBTs with an effective emitter junction area of 4.8 µm^2 exhibited peak f_T and f_{MAX} values of 265 and 305 GHz, respectively, at a collector current density of 3.75 mA/µm^2. Using this technology, a set of basic analog and digital IC building blocks, including lumped amplifiers, voltage controlled oscillators, multiplexers and demultiplexers, suitable for operation at 40 Gb/s and beyond, have been successfully designed and fabricated.**

I. INTRODUCTION

In the optical fibre telecommunications market, 10 Gb/s systems (OC-192) have now a large market share, whereas 40 Gb/s systems (OC-768) have been delayed and have not yet materialized. There has been, nevertheless, a continuously growing interest in high frequency devices. Hence, operation frequencies up to 200 GHz and even higher, have been reported, using different technologies, including GaAs- / InP-HEMTs (high electron mobility transistors) and SiGe- / InP-HBTs (heterojunction bipolar transistors) [1-4].

Prospective applications for these devices are high speed RF and mixed signal integrated circuits (ICs) for signal processing and next generation communications systems, operating at data rates of 80 Gb/s and beyond [5-8]. Lower frequency applications, however, could also benefit from this level of device performance for better signal quality and lower power implementation.

Hence, a considerable work related to the design and fabrication of high bandwidth, high speed mixed signal circuits, has been carried out using the above-mentioned technologies. In contrast to their contenders, InP-based HBTs combine, however, high operation frequency, high breakdown voltage, good uniformity and reliability, as well as the possibility of monolithic integration with 1.5 µm band photodiodes and optical modulators.

In this paper, we report the development of a manufacturable InP DHBT-based technology, suitable for medium scale mixed-signal and monolithic microwave ICs. Using this technology, a set of mixed-signal IC building blocks for ≥ 40 Gb/s fibre optical links, including lumped amplifiers, voltage controlled oscillators (VCO), multiplexers (MUX) and demultiplexers (DEMUX), have been successfully fabricated and tested above 40 Gb/s.

II. DEVICE STRUCTURE AND FABRICATION PROCESS

The InP DHBT layer structures were grown on 3" semi-insulating InP substrates, in a multiwafer (7x3") solid phosphorus molecular beam epitaxy (GEN-200). These structures feature an InP emitter, a graded carbon-doped InGaAs base (30 nm, 5x10^{19} cm^{-3}), and a composite InGaAs/InGaAsP/InP collector to minimize the collector current blocking effect.

The fabrication process of the InP DHBT-based ICs is based on conventional lithography using self-aligned base-emitter contacts and selective wet chemical etching. A benzocyclobutene (BCB) polymer film is used for device passivation and planarization.

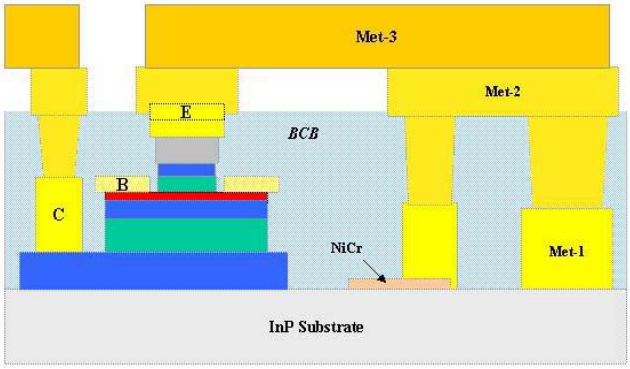

Fig. 1. Schematic cross-section of InP-based DHBTs technology.

The IC process is completed by NiCr resistors, thin film MIM capacitors and three levels of Au-based interconnect metals. Fig. 1 shows a schematic cross-section of the technology. Using this process, InGaAs/InP DHBTs have been manufactured with high yield and uniformity.

III. DEVICE CHARACTERISTICS

Fig. 2 shows typical Gummel plots of 1x8 µm^2 emitter size InGaAs/InP DHBTs. These devices displayed low leakage currents and a maximum current gain of $\beta \sim 85$. The collector and base ideality factors (n_C and n_B) were 1.1 and 1.45, respectively. The InP DHBTs exhibited also very uniform turn-on offset voltages of 0.12 V and breakdown voltages $BV_{CEo} > 5$ V.

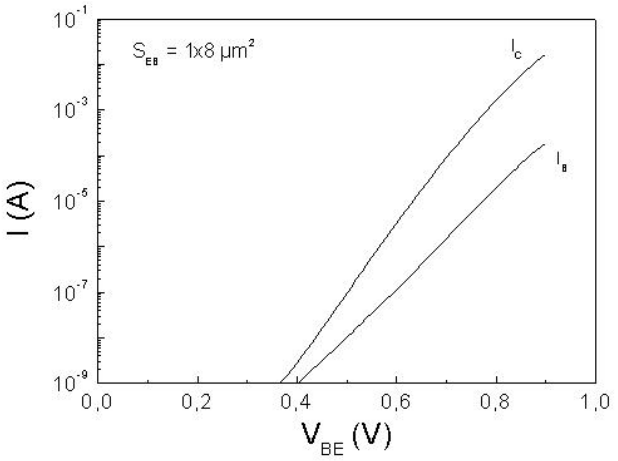

Fig. 2: Typical Gummel-plots of InGaAs/InP DHBTs.

A typical frequency dependence of the current gain (h_{21}) and unilateral power gain (Gu), of a 1x8 µm² device, is shown in Fig. 3. Using a -20 dB/decade extrapolation (dotted lines), a cut-off frequency (f_t) of 265 GHz and a maximum oscillation frequency (f_{max}) of 305 GHz were measured at a collector current (I_C) of 18 mA and a collector-emitter voltage (V_{CE}) of 1.5 V.

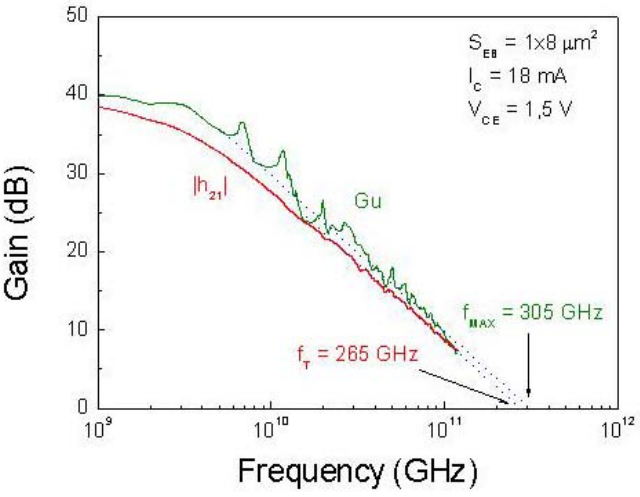

Fig.3: RF-properties of 1x8 µm² InGaAs/InP DHBT.

IV. CIRCUITS PERFORMANCE

Using this technology, an InP DHBT-based lumped amplifier for 40 Gb/s operation has been designed and tested. The circuit consisted of three transistors, of which two have been connected using the Darlington-configuration and the third one acts as a preamplifier stage. The circuit is matched to a 50 Ω environment. A chip micrograph of the DHBT-based amplifier is shown in Fig. 4.

Fig. 5 shows the amplifiers measured (solid lines) and simulated (dashed lines) S-parameters. The simulated data were obtained from a small signal model. The amplifier is characterized by a 3-dB bandwidth of 43 GHz and a gain of 19 dB. The bandwidth roll-off is very gradual, remaining over 10 dB up to 60 GHz. A -10 dB matching is obtained for the full bandwidth.

Fig. 6 shows the on-wafer measured 40 Gb/s amplifier's electrical eye diagram. The signal gain is 19 dB. The noisy pattern of the reference signal is caused by limitations in the oscilloscope. The amplifier signal shows a very clear eye and a voltage swing of approximately 600 mV. The circuit has a power consumption of 170 mW, when operated with a supply voltage of V_{CC} = + 6 V. This amplifier is well suited to be used in optical receivers.

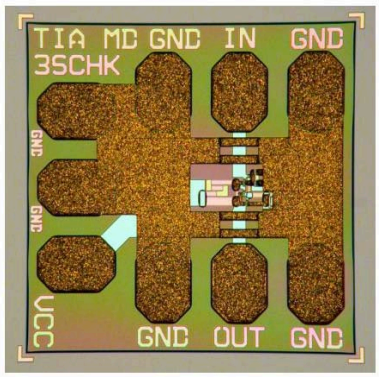

Fig.4: Chip photograph of an InP DHBT-based lumped amplifier. Chip-size: 0.5x0.5 mm²

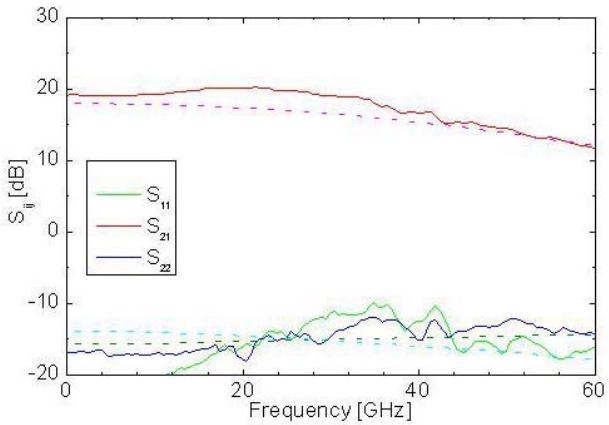

Fig.5: On wafer measured frequency response of an InP DHBT-based lumped amplifier.

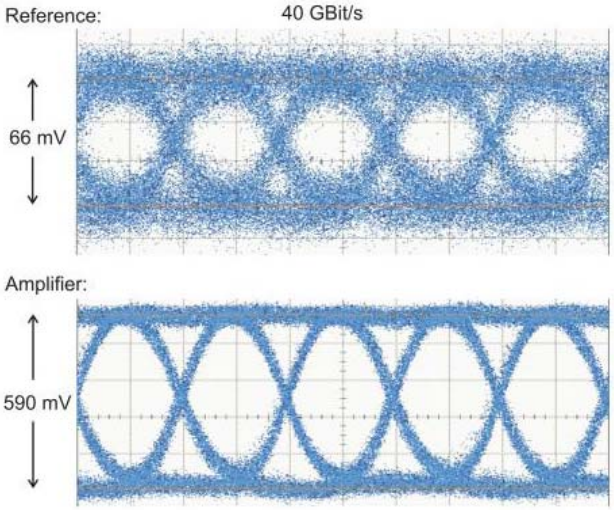

Fig.6: On wafer measured 40 Gb/s amplifiers eye diagram.

In addition, we have designed and fabricated 40 GHz VCOs, suitable as frequency sources for full-rate 40 Gb/s and half-rate 80 Gb/s mixed signal components, such as clock and data recovery (CDR) circuits. Fig. 7 shows the chip photograph of the realized VCO. The Chip size is 1.25 x 1.25 mm², while most of the chip area results from the measurement pads.

The oscillator's concept is based on a differential Colpitts-type configuration, which is extended by a cascode stage to ensure a full decoupling between the VCO core and the external load. More details have been reported elsewhere [9].

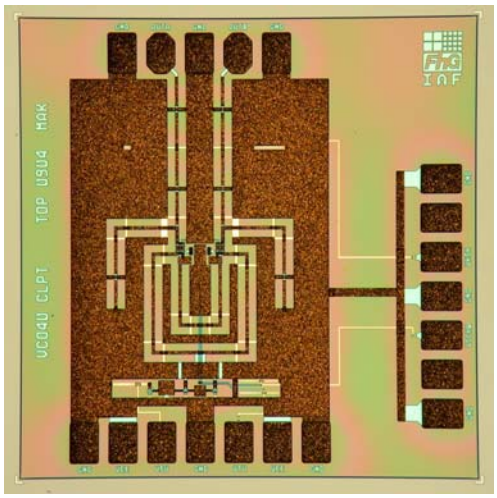

Fig.7: Chip photograph of the InP-DHBT-based VCO.

By varying the tuning voltage over 3 V, the VCO can be continuously swept from 39.5 GHz to 47 GHz, thereby showing a single-ended output power up to 3 dBm, i.e. a total signal power of 6 dBm. At 45 GHz, a minimum phase noise of – 108 dBc/Hz at 1 MHz offset frequency is achieved. The circuit features a power consumption of 136 mW, at a supply voltage of – 4 V. The spectrum of the VCO output signal at 45 GHz, is shown in Fig. 8.

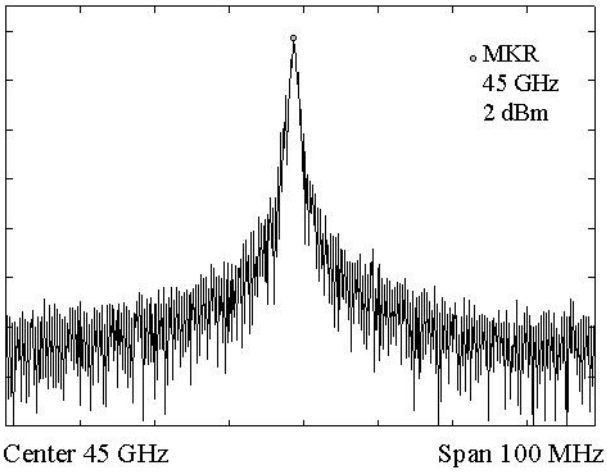

Fig.8: Output-spectrum of an InP-DHBT-based VCO at 45 GHz.

To further evaluate this technology, a 2:1 multiplexer core including three two-stage input drivers and a one-stage output driver has also been realized (Fig. 9). The inputs and outputs are implemented in differential circuitry. The circuit comprises 90 transistors.

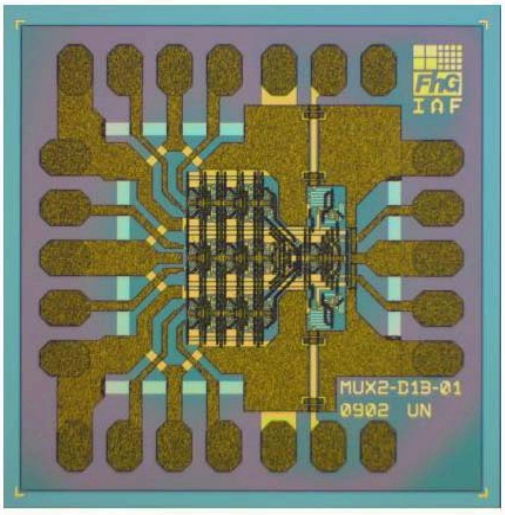

Fig.9: Chip-photo of the 50 Gbit/s multiplexer circuit. The chip size is 1x1 mm².

The multiplexer has been successfully tested at data rates up to 50 Gb/s, as shown in Fig. 10. The supply current is about 180 mA at 6.5 V supply voltage. The required input voltage swing is 200 mV in single-ended operation. The output signal voltage swing of the circuit is about 500 mV into a 50 Ω load.

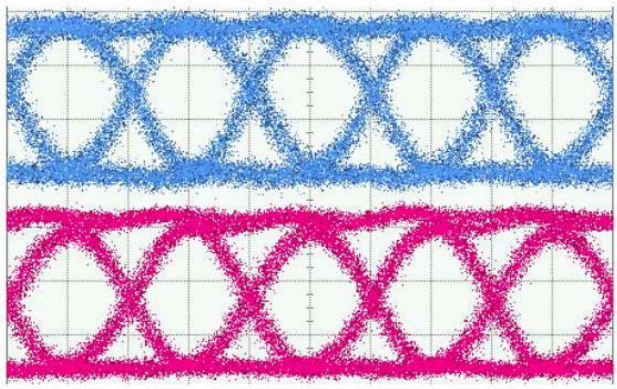

Fig.10: Output signal eye-diagram of the 50 Gbit/s multiplexer circuit.

Finally, a 1:2 demultiplexer (DEMUX) has been designed (ECL-technology) and successfully manufactured. The IC requires supply voltages of V_{EE} = - 4.5 V and V_{CC} = + 1 V and is able to drive 50-Ω loads. The circuit contains approximately 200 active components. The circuit has been tested with a data stream of 40 Gb/s and a clock frequency of 20 GHz. The DEMUX needs a single ended input data signal of ~ 600 mV_{pp}. The required single ended clock signal amounts to > 200 mV_{pp}. The total power consumption of this circuit is approx. 1.8 W.

A chip photograph and the eye diagrams of the 1:2 DEMUX outputs at an input data rate of 40 Gb/s are shown in figures 11 and 12, respectively.

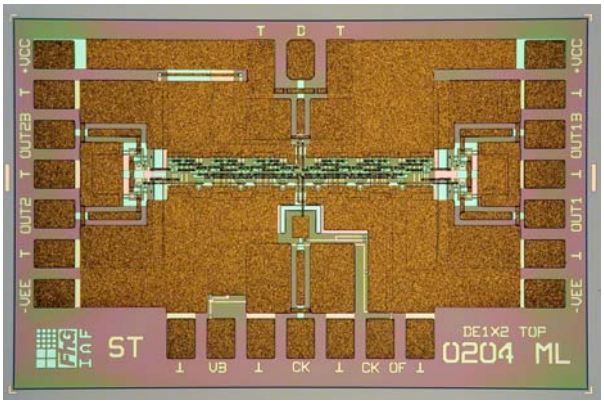

Fig.11: Chip-photo of the 40 Gbit/s 1:2 demultiplexer circuit. The chip size is 1.5x1 mm².

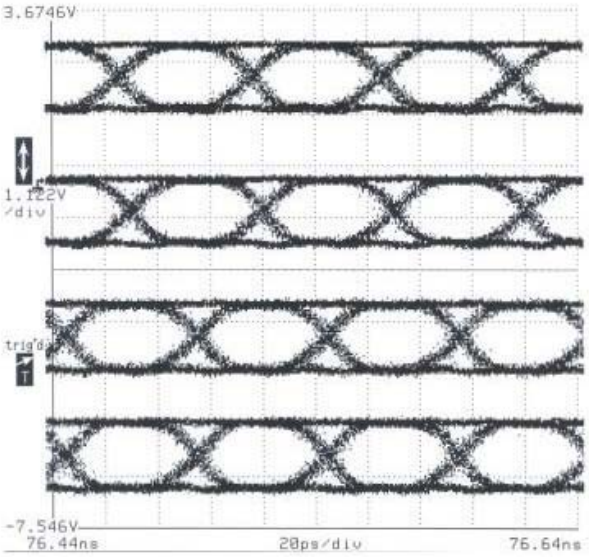

Fig.12: Eye diagram of the output signals of the 40 Gbit/s 1:2 demultiplexer circuit.

VI. Conclusion

In summary, the development of a manufacturable InP DHBT technology, suitable for medium scale mixed-signal and monolithic microwave ICs, has been reported. A set of mixed-signal IC building blocks for ≥ 40 Gb/s fibre optical links, including lumped amplifiers, voltage controlled oscillators (VCO), multiplexers (MUX) and demultiplexers (DEMUX), have been successfully fabricated and tested above 40 Gb/s.

These results confirm the great potential of InP-based DHBTs, and hold great promise for future optical communication systems. The development of higher bit rate mixed signal ICs is in progress. The simulation results indicate that over 80 Gb/s ICs should be achievable using the present technology.

Acknowledgement

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References

[1] K. Shinohara, T. Matsui, Y. Yamashita, A. Endoh, K. Hikosaka, T. Mimura, I. Watanabe, S. Hiyamizu: 'HEMTs with ultrahigh cutoff frequency' International Symposium on Compound Semiconductors: San Diego CA, USA, p 124-31, Aug. 2003

[2] Z. Griffith, M. Dahlstrom, M.J.W Rodwell, X.M. Fang, D. Lubyshev, Y. Wu, J.M Fastenau, W.K Liu : 'InGaAs-InP DHBTs for increased digital IC bandwidth having a 391-GHz f(t) and 505-GHz f(max)' IEEE Electron Device Letters, 26 (1), p 11-13, 2005

[3] M. Ida, K. Kurishima, K. Ishii, N. Watanabe: '3.48 ps ECL ring oscillator using over-300 GHz f(T)/f(max) InP DHBTs' Electronics Letters, 39 (16), p 1215-17, (2003)

[4] G. Freeman, B. Jagannathan, J.J. Shwu, S.R. Jae, A.D. Stricker, D.C. Ahlgren, S. Subbanna: 'Transistor design and application considerations for >200-GHz SiGe HBTs' IEEE Transactions on Electron Devices, USA * vol 50 (March 2003), no 3, p 645-55

[5] K. Murata, K. Sano, T. Enoki, H. Sugahara, M. Tokumitsu: 'InP-based IC technologies for 100-Gbit/s and beyond' International Conference on Indium Phosphide and Related Materials. Kagoshima, 31 May-4 June 2004, p 10-15, 2004 International Conference on Indium Phosphide and Related Materials. 16th IPRM, Kagoshima, Japan, 31 May-4 June 2004 * Piscataway, NJ, USA: IEEE, 2004, p 10-15

[6] A. Konczykowska, P. Andre, F. Jorge, J. Godin: 'High quality 80Gbit/s InP DHBT selector and its use for NRZ-RZ conversion' Electronics Letters, 39 (1), p 49-51, 2003

[7] M. Meghelli, A.V Rylyakov, S.J Zier, M. Sorna, D. Friedman, "A 0.18-µm SiGe BiCMOS receiver and transmitter chipset for SONET OC-768 transmission systems," IEEE Journal of Solid-State Circuits, 38 (12), pp. 2147-2154, 2003.

[8] Y. Baeyens, G. Georgiou, J.S. Weiner, A. Leven, V. Houtsma, P. Paschke, Q. Lee, R.F. Kopf, Y. Yang, L. Chua, C. Chen, C.T Liu, Y.K. Chen, „InP D-HBT ICs for 40-Gb/s and higher bitrate lightwave transceivers" IEEE J. Sol. State Circuits, 37 (9), p 1152-1159, 2002

[9] R. E. Makon, K. Schneider, R. Driad, M. Lang, R. Aidam, R. Quay, G. Weimann: 'Fundamental low phase noise InP-based DHBT VCOs with high output power operating up to 75 GHz', Proc. 2004 Compound Semiconductor IC Symposium, Monterey, pp. 159–162, October 2004.