A silicon-like process for high volume and low cost GaAs MMICs

D. Pons#
ums

A GaAs MESFET process has been established for high volume and low-cost production of RF or microwave monolithic integrated circuits for wireless communication applications.

The main features of this process are as follows : a field oxide layer is deposited on the whole surface of the semi-insulating substrate. The active chanel of the MESFET is defined by a local Si implantation into a window opened through this field oxide. The ohmic source and drain contacts are self-aligned by Si implantation, using the W-based gate as a mask. Up to three interconnect levels are available. The whole process avoids completely the use of gold : the gate metal is sputtered and etched (0.7µm); the GeNi ohmic contacts are evaporated and lifted ; Al is used for the interconnect layers.

Three different implantation profiles have been optimized for the realization of three different transistors : normally-off (E), normally-on (D) and power MESFETs. All three MESFETs can be combined in a circuit, the E/D pair for low consumption control functions and the third one for power amplifiers. The main electrical characteristics of these transistors are given in the following table.

	norm. - ON	norm. - OFF	Power
Idss (mA/mm)	150	40	250
Vth (V)	-0.85	+0.2	-2.3
Gm (mS/mm)	330	280	200
Ft/Fmax (GHz)	25/45	23/40	17/22
Fmin/Gass (dB) @ 2 GHz	0.6/16	0.6/15	-
Pout (mW/mm)	-	-	310

This process, called SA70 (for Self-aligned, Lg = 0.7µm), is run on a modern 4" line with a high volume and throughput capability.

Several examples of circuits which have been developed with this process for various wireless communication applications will be detailed, including GSM low voltage (3V) high power amplifiers, a DECT RF front-end circuit and a chip-set for an automatic road tolling system at 5.8 GHz.

United Monolithic Semiconductors, **ums SAS**, 91401 Orsay Cedex (France)