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A Comprehensive Model Verification Procedure for General-Purpose Microwave FET Models

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INTRODUCTION

Model validation represents a very important step in the complex process of device modelling. In theory, an ideal verification strategy should contain the necessary and sufficient number of tests, which could prove the validity of the model in all applications that it is intended to be used for. Consequently, the wider the range of applications for a certain model, the higher and more complex the number of validation tests needed. Unjustifiably, this issue has been generally sidelined, in the sense that most validation procedures, have consisted in a reduced, non-sufficient set of tests. Only recently, a few research groups have began to stress the importance of the entire validation process and to look for more comprehensive approaches [1,2,3].

A recent survey carried out among microwave CAD users (including large GaAs foundries), have identified the following important general specifications for non-linear FET models: *(i)* models should be as general-purpose as possible; *(ii)* models should be scaleable; *(iii)* models should be easy-to-use and robust. In this contribution we do not concentrate on the solutions to achieve these goals, but on setting out an optimum model verification procedure that should be followed in order to prove that an already developed model meets these requirements.

Consistently in the past, validation tests presented in literature for various models consisted in DC, small-signal and/or single-tone large-signal tests performed in a 50Ω environment for one or two bias conditions and showing, in general, good agreement between simulation and measurement. It is well accepted at present that such a procedure can not guarantee the validity of a model in other different operation conditions. The main reasons being: *(a)* the limitations induced by a 50Ω test environment, specially for the large-signal tests and *(b)* the lack of specific tests to prove the model's ability to reproduce complex higher-order effects (low-frequency dispersion, intermodulation products, etc.). Although a sufficient verification procedure could probably be imagined, in reality one has to settle for a practically feasible solution. Such a solution should contain a limited number of tests (which would require generally-available test equipment) covering, as fully as possible, the operation conditions encountered in the range of applications where a particular model is intended to be used.

In this paper we outline the validation procedure that we have implemented for the verification of the scaleable, general-purpose *COBRA* model for FETs. Finally, we present results from some of the tests carried out so far.

MODEL VERIFICATION PROCEDURE

A comprehensive model verification procedure has been considered in order to test the scaleable, general-purpose *COBRA* model. This procedure includes:

- regular DC tests over the entire bias spectrum (input and output DC *I-V* characteristics);
- low-frequency pulsed tests;
- small-signal broad-band S-parameter tests for at least five different bias conditions, spread around the entire bias plane as follows (see Figures 1 and 2):
    1. *Vgs* at pinch-off and *Vds* in linear region
    2. *Vgs* at pinch-off and *Vds* in the soft breakdown region
    3. *Vgs* and *Vds* in the mid-bias range (approx. *Idss/2*)
    4. $Vgs \cong 0$ and *Vds* around the knee region
    5. $Vgs \cong 0$ and *Vds* well in the saturation region (approx. *Idss*);
- 50 ohm single-tone large signal tests for the same five bias points and for a couple of different frequencies. The devices should be driven well beyond the 1dB compression point and the output signal will be monitored up to at least the third harmonic;
- 50 ohms two-tone large-signal tests for the five bias conditions. The devices should be driven well into compression and at the output, the two fundamental components plus the third order intermodulation products should be monitored;

- all the above tests should be repeated for a number of representative device sizes (at least three different device sizes) in order to test the scaling capabilities of the model.

In practice, pulsed and intermodulation characteristics are the most difficult to obtain, mainly because the corresponding measurements require more sophisticated and expensive equipment. If such experimental data is not available, alternative simulation tests can be carried out in order to prove the model's capabilities in those areas (although to a lesser extent), such as the prediction of bias variation for the main small-signal intrinsic elements, prediction of different *I-V* output characteristics under DC and pulsed conditions, and predicting the right type of behaviour for the 1^{st}, 2^{nd} and 3^{rd} derivatives of the drain current function used in the model [4].

VALIDATION RESULTS IN THE CASE OF *COBRA* MODEL

The verification procedure described above has been applied to test the *COBRA* FET model, for both MESFET and PHEMT devices, and within the limited space of this paper, some of those results are included below. In Figure 3 the DC test results are presented for a 120μm PHEMT and then scaled to a 300μm PHEMT. In Figure 4, we show results from small-signal S-parameter tests for a 120μm PHEMT at eight different bias points, including extreme bias conditions such as the "unbiased" and deep "pinched-off" device. In Figure 5, we see results from a similar test, at three different bias points, with the model scaled to a 300μm PHEMT from the same process. Further, in Figure 6, single-tone large-signal test results are presented for four different bias conditions, for the 120μm PHEMT. Figure 7 shows the capability of the model to predict different output characteristics under DC and low-frequency pulsed conditions. Finally, in Figure 8 we show the results from an IM3 test performed on a 0.5x300μm GaAs MESFET. The input level of the 5.00GHz signal has been kept constant at +10dBm, while the level of the 5.01GHz signal was swept from -15dBm to +15dBm.

CONCLUSIONS. ACKNOWLEDGEMENTS

We have outlined the procedure that we have implemented for the validation of the scaleable, general-purpose *COBRA* model for microwave FETs. We presented a significant number of the test results carried out so far, including DC, pulsed, small-signal, single-tone and two-tone large-signal, as well as scaleability tests.

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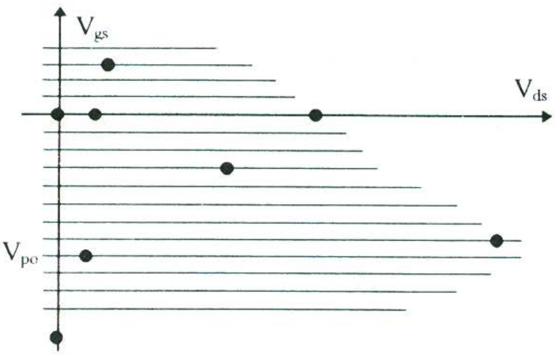

Figure 1. Distribution of the bias points selected for model verification tests around the *Vgs-Vds* bias plane

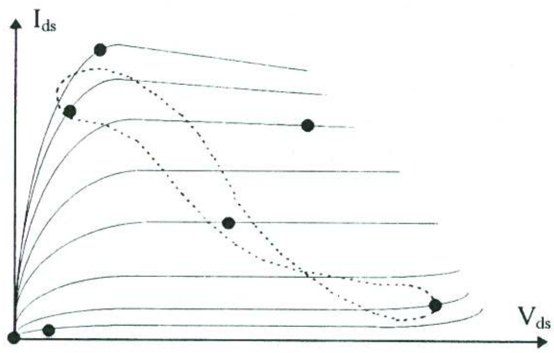

Figure 2. Distribution of the selected test bias-points around the *I-V* characteristics with a typical 50 Ω load-line

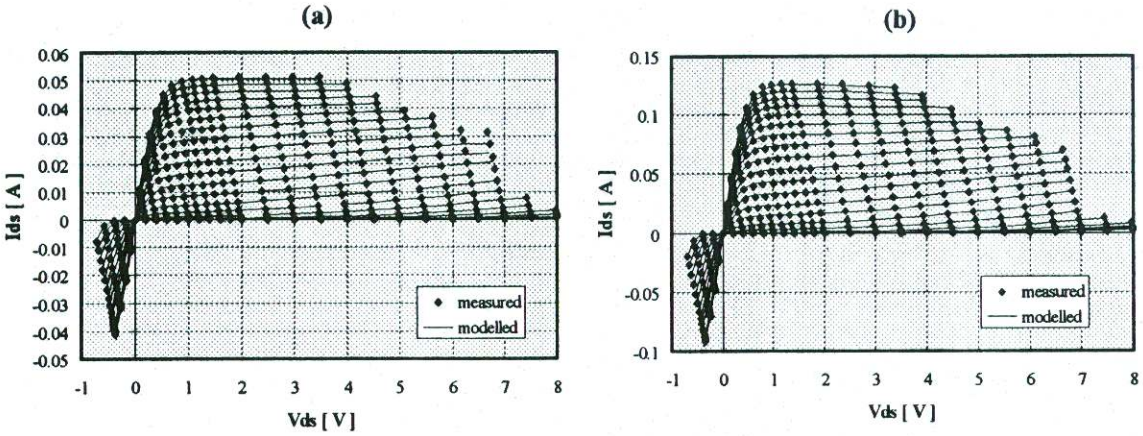

Figure 3. Scaleable *COBRA* DC model applied to a 120μm **(a)** and to a 300μm **(b)** PHEMT (V_{po} = *- 1.0 V*)

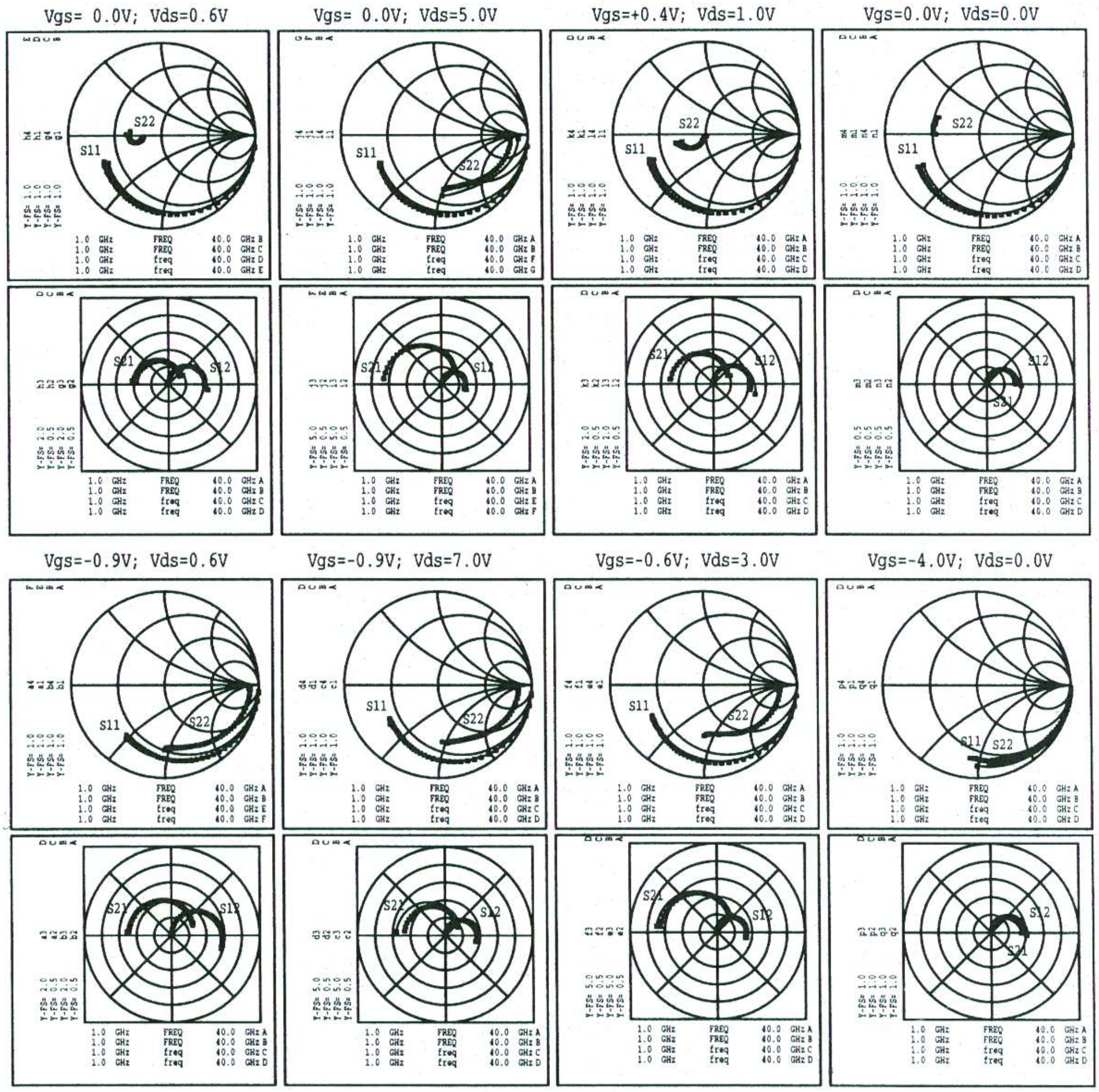

Figure 4. Multi-bias, small-signal S-parameter validation test of *COBRA* model for a 0.2x120μm PHEMT (measurement - *dots*, simulation - *continuous lines*)

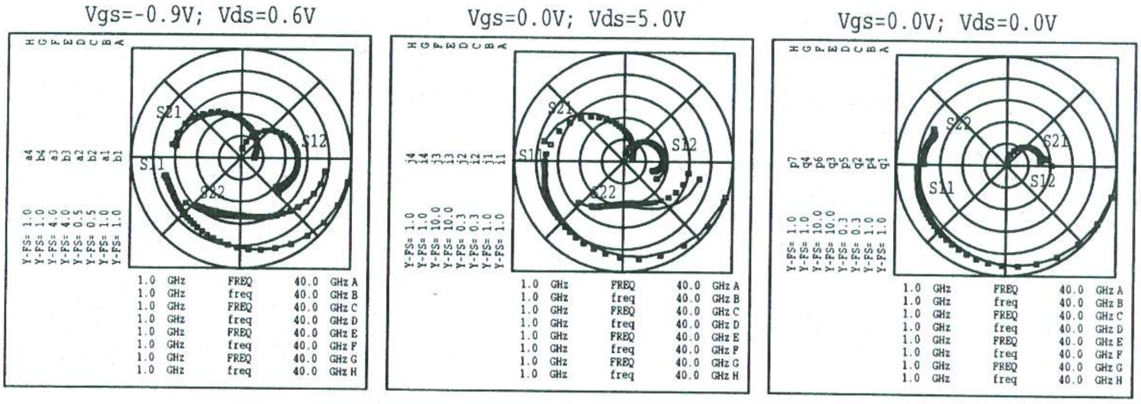

Figure 5. S-parameter validation test of *COBRA* model for a 300μm PHEMT (scaled from 120μm) (measurement - *dots*, simulation - *continuous lines*)

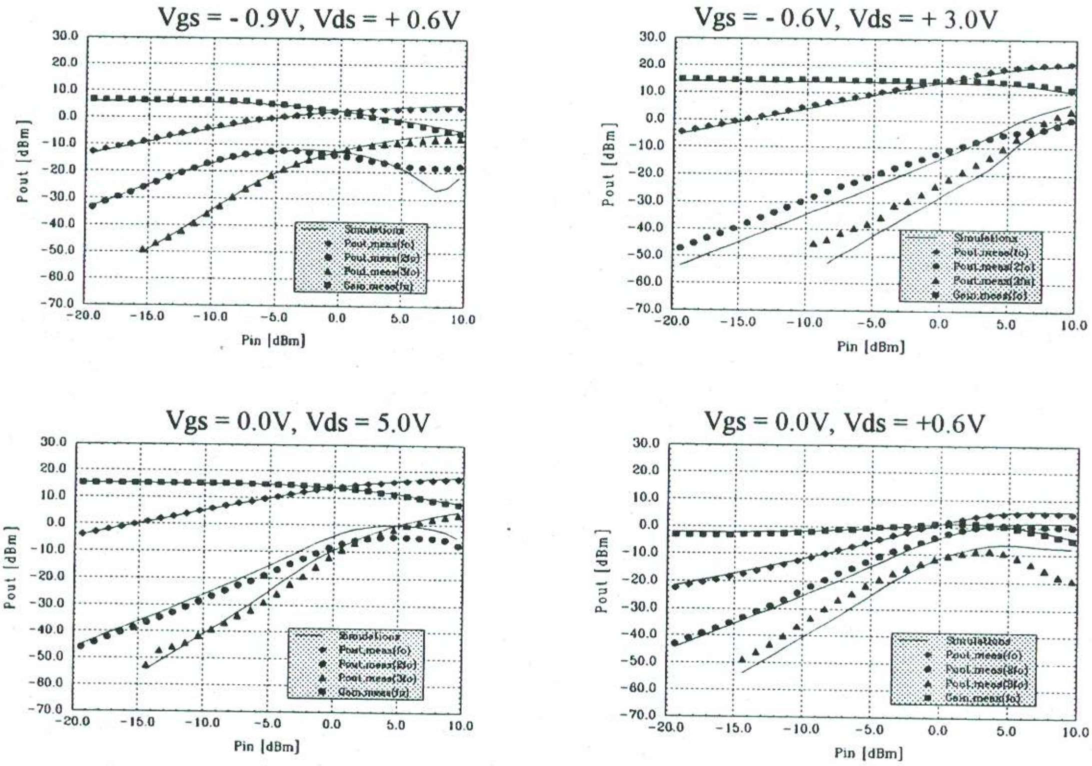

Figure 6. Single-tone large-signal tests performed with *COBRA* model for a 300μm PHEMT

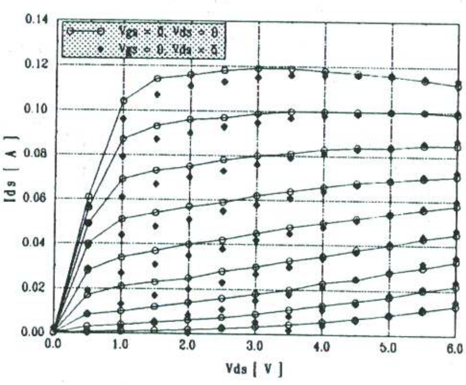

Figure 7. Pulsed characteristics simulated with *COBRA* in MDS for two different quiescent points

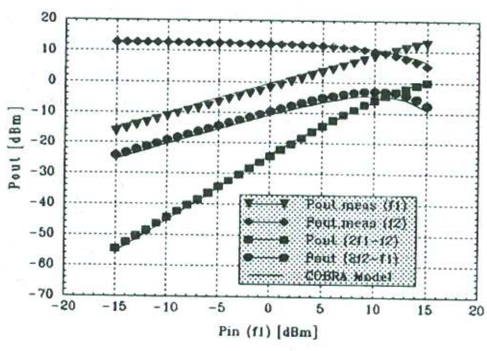

Figure 8. IM3 test carried out on a 0.5x300μm MESFET (f_1 = 5.00GHz, f_2 = 5.01GHz; V_{gs} = -1.0V, V_{ds} = 3.0V)