

# A Low-Noise, High-Linearity Balanced Amplifier in Enhancement-mode GaAs pHEMT Technology for Wireless Base-Stations

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**Abstract** — This paper describes the design and realization of a balanced low-noise amplifier (LNA) module in the 2GHz band suitable for wireless infrastructure (base-station) receiver front-end applications. The design effort entails both aspects of MMIC and module/package design to realize a fully-matched solution in a miniature 5mmx6mm footprint. The MMIC design leverages Agilent Technologies' proprietary 0.5 micron enhancement-mode Pseudomorphic High-Electron-Mobility Transistor (e-pHEMT) technology for best-in-class noise performance and linearity. In a balanced amplifier application with external 3-dB hybrids, this design exhibits a very low noise figure (NF) of 0.9dB, coupled with a high OIP3 (Output Third Order Intercept Point) of 46dBm at 31dB gain. It is also capable of delivering a P-1dB of 31dBm at 2.0GHz with a 5.0V supply.

## I. INTRODUCTION

Designers of wireless base-station circuits face increasing challenges in terms of size, cost and design cycle-time without compromising the stringent requirements imposed on them. For example, Tower-Mounted Amplifiers (TMA) and Receiver Front Ends must meet the duality of low NF (<1dB) and high OIP3 ( $\geq 45$ dBm). In addition, these amplifiers have to be load- and source-insensitive, meaning that the input and output return losses have to be 20dB or better. To achieve this, such amplifiers are typically balanced amplifiers employing hybrid couplers [1]. Although there are many solutions in the market capable of meeting these requirements, they typically are multi-stage designs using many discrete components thus requiring much engineering effort to realize. At Agilent Technologies, significant progress has been made in overcoming the low noise-vs-linearity-vs-efficiency conundrum through a proprietary 0.5 $\mu$ m GaAs e-pHEMT process [2]. This paper demonstrates that with appropriate device sizing, biasing and matching at the die level and in combination with a few miniature surface-mount discrete components in an encapsulated chip-on-board (COB) package, an extremely low-noise, high-linearity, high-power amplifier can be designed without resorting to fancy and complicated circuitries. The result is an easy-to-use module measuring 5x6x1.1mm<sup>3</sup> requiring only external 3-dB hybrid couplers and some external standard decoupling capacitors.

## II. BALANCED AMPLIFIER DESIGN PHILOSOPHY

Figure 1 shows the simplified diagram of the balanced amplifier module. Basically the topology consists of two identical mirror-imaged amplifier chains, each having two amplifying stages. The first (input) stage is a high-gain, low noise amplifier, which determines the NF, while the second (output) stage delivers the power and determines the overall OIP3. The amplifier stages and associated bias and matching components are all contained within the module. The 3-dB hybrid couplers are connected externally. The advantage of such a design is the flexibility it affords to the user in the choice of couplers for reasons of cost, size and performance (especially the insertion loss). In some applications, users may use the (single-ended) amplifiers independently.

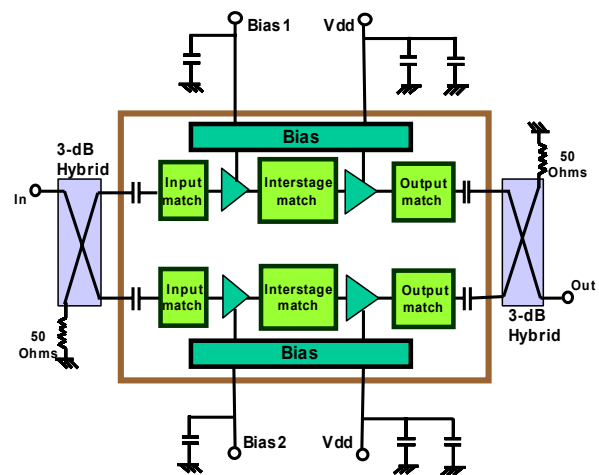


Fig. 1. Block diagram of the balanced amplifier

## III. THE DIE-LEVEL AMPLIFIER DESIGN

Figure 2 shows the simplified schematic of each amplifier chain within the module. As indicated, each amplifier chain consists of an on-chip section and some off-chip discrete (surface-mount) passive components. The Agilent Technologies Advanced Design System (ADS) simulator was used extensively to predict and

optimize the small-signal and non-linear performance of each amplifier stage during the design phase. The simulation schematic for the amplifier stages is shown in Figs. 3 and 4. Agilent's proprietary non-linear, small-signal and noise models for the FETs were used to ensure accurate simulation results. The transistor (FET) Q1 is connected as a conventional common-source amplifier and input-matched using a high-Q wirewound shunt inductor for the best NF. This is followed by a series coupling capacitor to the gate of Q1. The latter is sized at 800um to give 16dB of gain.

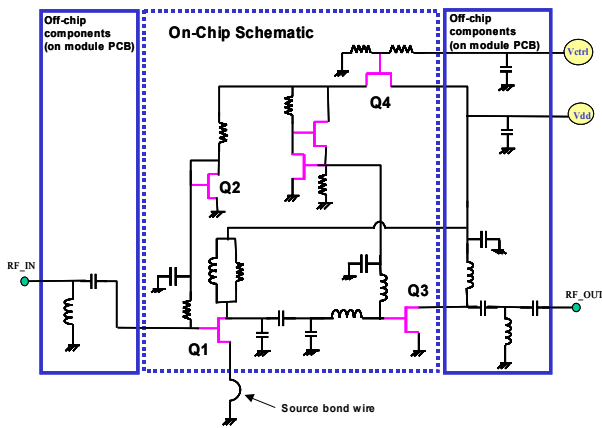


Fig. 2. Simplified schematic of each amplifier chain.

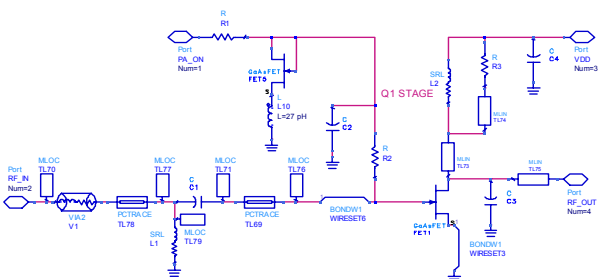


Fig. 3. Simulation schematic of the first stage amplifier.

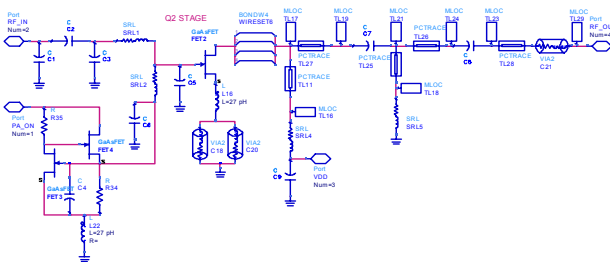


Fig. 4. Simulation schematic of the second stage amplifier.

Since the amplifiers will be used in balanced configuration the input matching inductor is selected not for optimum return loss, but for best NF. Source tuning is featured as it affords easier input matching as close to  $F_{min}$  as possible (see Fig. 5). Being a low-noise high-gain stage, extreme care is needed to stabilize the device without compromising NF. In this respect the amount of source inductance, which is provided by a bond wire,

must be carefully chosen. Stabilization is achieved by means of a resistor-loaded inductor at the output of Q1. The gate bias for Q1 is provided via a diode-connected current mirror FET Q2. The size of Q2 is carefully chosen for its noise contribution and current delivery to the gate of Q1. Noise from Q2 is mitigated by appropriate choice of a shunt capacitor and isolating resistor at the gate of Q1. The value of the isolating resistor must be big enough to block the noise, yet small enough to not add significant thermal noise into Q1. The value of the resistor is also critical in setting the P1-dB of Q1 to effectively drive Q3. Through simulation, a 10k-ohm resistor was found to be appropriate.

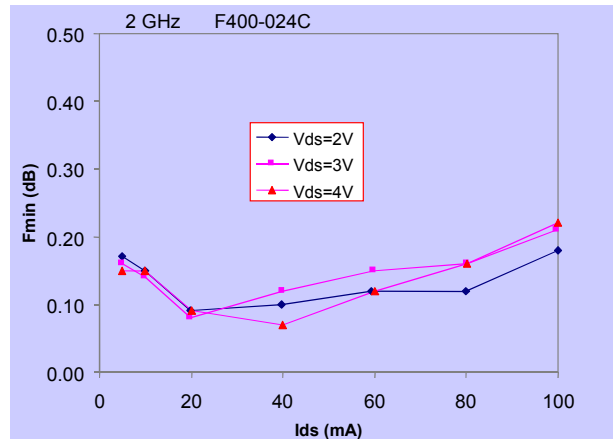


Fig. 5.  $F_{min}$  vs  $I_{ds}$  and  $V_{ds}$  of a 800um FET in Agilent's 0.5um GaAs E-pHEMT process

The output FET Q3 is also connected as a common – source amplifier. It is sized at 6400um to give at least 27dBm of OP1-dB, 45dBm of OIP3 and 15dB of gain. Unlike Q1, the source of Q3 is hard-grounded using vias for optimum gain and power output performance. The bias circuit for Q3 consists of a dual-pHEMT self-compensating current source [3]. The output matching for Q3 is of a high-pass configuration to kill low-frequency gain to maintain stability in that region. All the inter-stage matching between Q1 and Q3 are located on-chip. A CMOS-compatible switch Q4 enables independent switching/control of either amplifier chain. The simulated performance of each amplifier chain is shown in Figs. 8 to 11.

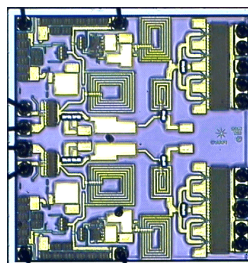


Fig. 6. Photomicrograph of the actual MMIC. The die occupies an area of 2.75mm<sup>2</sup>.

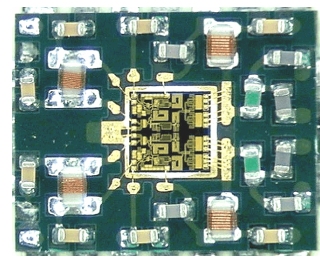


Fig. 7. PCB layout of the module showing the MMIC and discrete components.

Figure 6 shows the layout of the MMIC in Agilent's proprietary 0.5um enhancement-mode GaAs-AlGaAs

pHEMT process. The fabrication uses molecular beam epitaxy (MBE) on 6" wafers. Being an enhancement-mode technology means that the device requires only positive voltage supplies thus doing away with the problematic power-up sequence required of (negative-gate-bias) depletion-mode types. Threshold voltage is about 0.4V with 550mS/mm transconductance, and a respectable  $f_T$  of about 30GHz. The extremely low Fmin in combination with high  $f_T$  at the die level enables the design of amplifiers with the duality of very low noise and high linearity.

#### IV. THE MODULE AND PACKAGING DESIGN

The simulation schematics in Figs. 3 and 4 also include packaging parasitics, i.e. bond wires, bond pads, board traces, component pads and via holes. The layout of the module is shown in Fig. 7. The PCB material is Getek®

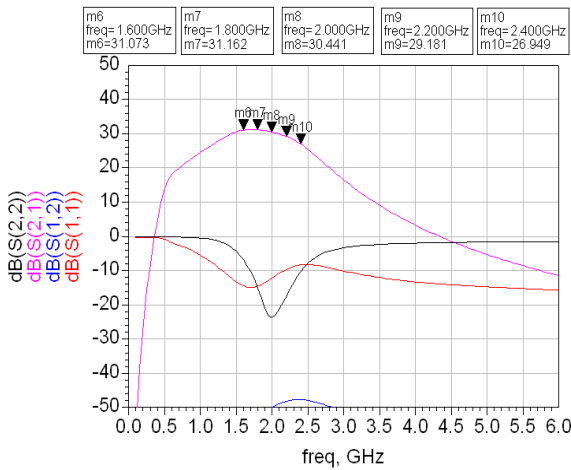


Fig. 8. S-parameter simulation results.

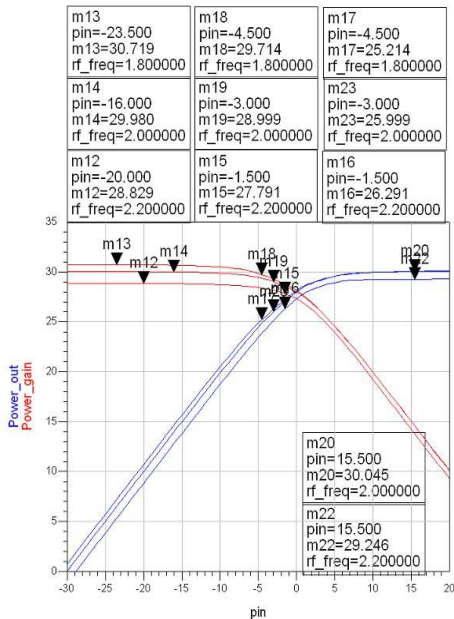


Fig. 9. Harmonic balance simulation results. with a dielectric constant of 3.9. It is imperative that the simulation effort be an on-going exercise to track

changes in the layout and design. As a result all critical electrical parameters were met after just one turn of wafer and module PCB fabrication! Figure 12 shows the final encapsulated module mounted on a Rogers® RO4350 evaluation demoboard with a dielectric constant of 3.48.

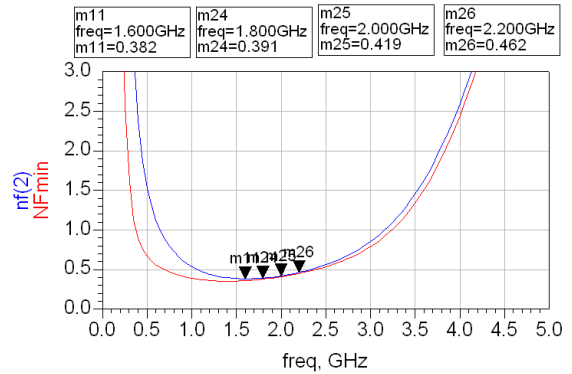


Fig. 10. Noise figure simulation.

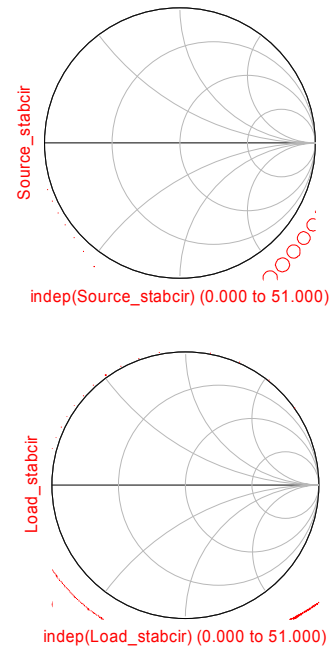


Fig. 11. Source and load stability circles to ensure stability of the design up to 20GHz.

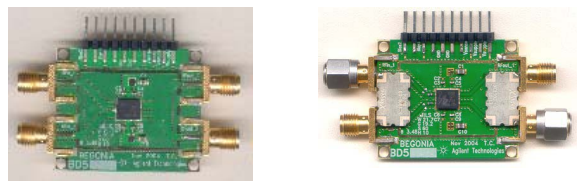


Fig. 12. The module mounted on demoboard for single-ended (left) and balanced (right) measurements.

For the balanced application, the 3dB quadrature hybrid couplers used here are Anaren®'s commercially available components with datasheet performance of 0.12dBmax insertion loss and >20dB return loss [4].

## V. MEASURED PERFORMANCE

The typical single-ended performance for each amplifier channel is shown below in Table 1. Fig. 13 shows the actual s-parameter plots.

Table 1 : Single-Ended Performance at 2GHz

Supply voltage:	5.0V
Small-signal Gain:	31dB
Noise Figure:	0.60dB
Psat/Current:	29.3dBm/340mA
OP-1dB/Current/PAE:	27.8dBm/309mA/39%
OIP3:	46dBm
Pout/Current @ OIP3:	15dBm/381mA
Input/Output Return Loss:	12dB/10dB

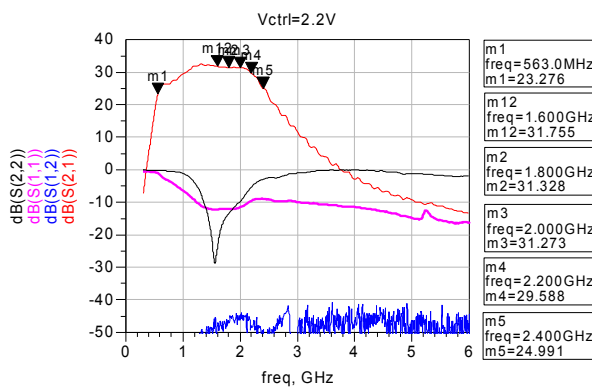


Fig. 13. S-parameter plots of actual single-ended performance.

Table 2. Summary of simulated vs actual performance over the design bandwidth of 1.8-2.2GHz

Parameter	Units	Simulated	Actual
<b>Noise Figure</b>	dB	0.4-0.5	0.5-0.65
<b>Gain</b>	dB	29-31	30-32
<b>P1dB</b>	dBm	25-26	27-29
<b>OIP3 - Fund power</b>	dBm	14-15.5	15
<b>- OIP3</b>	dBm	36-37	43-46
<b>Current</b>	mA	370	380-400
<b>Input RL</b>	dB	10-15	10-13
<b>Output RL</b>	dB	10-24	9-27

Table 2 shows the comparison between simulated and actual performance. Very good correlation was obtained for most parameters. Simulated noise figure is typically slightly more optimistic than actual due to unaccounted-for sources of noise such as the power supply, ambient radiation and package molding material. Simulated OIP3 is typically poorly correlated. When connected as a balanced amplifier, the overall performance depends on the quality of the hybrids used. Typical insertion loss ranges from 0.1dB to 0.3dB. At the input of the amplifier, this would cause a dB-for-dB degradation in the NF. At the output, due to the 3dB combining effect of the coupler, the OP-1dB and OIP3 should theoretically be increased by 3dB. Fig. 14 shows the s-parameter plots of

the balanced amplifier. The return losses have been improved by the hybrids over that of the single-ended performance, i.e. the S11 and S22 improved to about 19dB (at 2GHz) compared to 12 and 10dB respectively. Noise figure degraded to 0.9dB, which is more than the insertion loss (0.1dB) of the input coupler. The additional loss can be attributed to trace losses between the coupler and the module, and coupling between the two halves of the balanced amplifier due to non-optimum layout. The OP-1dB and OIP3 measured 31dBm and 46dBm respectively.

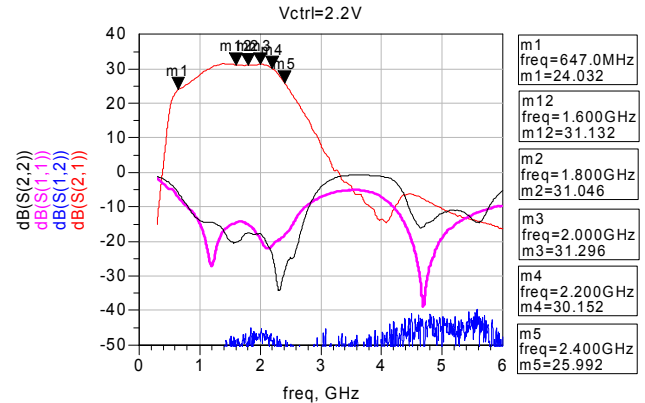


Fig. 14. S-Parameter plots for the balanced amplifier.

## VI. CONCLUSION

The design and measured performance of a low-noise, high-linearity, high-power amplifier module at 1.8-2.2GHz has been presented. At 2GHz, an extremely low NF of 0.6dB (single-ended) and 0.9dB (balanced) has been achieved, in addition to providing 46dBm of OIP3 and OP-1dB of 31dBm. With internal matching, an easy-to-use solution has been realized with a performance level meeting the stringent requirements of wireless base-station receiver front-end amplifiers. To our knowledge this represents a significant breakthrough in terms of performance, size, cost and convenience versus that of currently available solutions.

## ACKNOWLEDGEMENT

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