GAAS® 97 • 5th European Gallium Arsenide and related III-V compounds Applications Symposium
Bologna, Italy - September 3rd-5th, 1997

Full electrothermal characterization of GaAs FETs

S.Mons*, E.Ducloux**, E.Leclerc***, L.Thibaudeau**, R.Quéré*
* IRCOM UMR CNRS n°6615 IUT GEII 7 rue Jules Vallès 19100 Brive
** Thomson L.C.R. Domaine de Corbeville 91 Orsay
*** UMS Route Nationale 1278 91 Orsay

Abstract
An electrothermal characterization of GaAs MESFET has been performed using pulsed measurements. The measurement process has been realized under the same bias conditions at different temperatures of the device. It allows the determination of a nonlinear model at each temperature. Moreover the characterization method is based on the electrical measurement of the temperature channel. This specific measurement process under pulsed bias conditions allows to derive a full electrothermal nonlinear model representing the transistor self heating phenomena. The obtained values have been validated by a full three dimensional thermal simulation.

Introduction

Microwave power generation is of prime importance for a large number of applications either civilian or military. Thermal behavior of power circuits is a key point of the design process [1]. Indeed, because of self heating effects, the power results and the channel temperature must be simultaneously evaluated for an accurate prediction. Moreover, a predictive technique to determine the thermal behavior of multifinger power GaAs MESFET must be used in order to determine the optimum topology of the device. This technique requires to determine both the intrinsic electrothermal model of the active and the thermal embedding circuit (thermal resistance and capacitance). The thermal circuit determination can be performed either by numerical calculation by using three dimensional simulation [2] or thermal measurement [3]. In order to validate both method, a comparison has been performed between numerical 3D simulation and electrical measurements on a set of known devices. The aim of this paper is first to describe the electrothermal modeling technique based on pulsed measurements and to demonstrate the good agreement obtained with numerical 3D thermal simulation.

Numerical 3D simulation technique

We solve the thermal problem with software developed at Thomson -T.C.S.-L.C.R.. The temperature is computed by solving the stationnary equation: $\overrightarrow{\nabla} \cdot \left(k(x,y,z,T) \cdot \overrightarrow{\nabla} T(x,y,z) \right) + S(x,y,z,T) = 0$

where k(x,y,z,T) is the nonlinear thermal conductivity and S(x,y,z,T) is thermal source.
The boundary conditions are given by fixing the temperature T or by a null normal thermal flux condition.
The thermal resolution is performed by a 3D Finite Element method using P2 Lagrange tetrahedric elements. This leads to the inversion of a sparse linear system, which is done by direct or iterative methods, depending on the dimension of the problem. The non linearity is taken into account by a simple iterative procedure (fixed point method) which fits well the weak non linearity of the equation (less than 10 iterations are necessary to meet convergence).

Principle of an isothermal electrical characterization based on pulsed measurements at fixed trap level

When performing DC measurements, self heating effects make the intrinsic temperature vary when the control voltages are changed. Therefore it is not possible to separate thermal effects from thoses of the other comands in the transistor. So the acurate thermal characterization must be made under pulsed bias conditions: A pulsed I(V) and pulsed [S] parameter measurement system were used to characterize the electrothermal model by performing a set of isothermal measurements at various temperatures. The principle of the method is illustrated on the figure 1.

If we ensure that the pulse duration and duty cycle are smaller than the thermal time constant to avoid self heating effects during the pulses, then the thermal state of the device is fully controlled by the quiescent level of the bias voltage. Thus, we apply a large pulse to bias up the device from a quiescent level with no power dissipation. Moreover, to ensure that trap effects do not modify our thermal characterization, those measurements are performed at constant Vds bias voltage which is the first responsible of trapping effect variations. This measurement technique allows to perform a set of isothermal measurements so that all of the required data for a single device at a single temperature are stored in one file for reading by modeling programs. In order to be efficient, this setup is fully computer controlled. The software takes care of the device limits and automatically traces I-V and diode characteristics. An open database structure has been defined providing a direct interface to the modeling activity. Moreover, for thermal characterization, this setup is coupled with a thermal enclosure and all measurements are made without device disconnection. In this configuration where there is no dissipated power, the temperature measured in the thermal enclosure at the level of the device is then signifiant of the thermal state of the test vehicle.This characterization process has been performed by using the test kit WILTRON 36380K up to 20 Ghz. The results presented in this paper concern five characterizations from the the ambiant temperature up to 100°C. The chip lays on a brass stand whose measured temperature with a probe will be used as a reference.

Determination of the nonlinear electrothermal model

We perform simultanously pulsed I(V) and S-parameter measurements of device characteristics at various temperatures with no DC power dissipation so that we obtain the variation of the nonlinear model as a function of

temperature. Then, a nonlinear model can be extracted with fitting every parameters of each nonlinearity determined at the fixed temperature T_i From these measurement results stored in a data base, one can extract the variation of temperature coefficients for each nonlinear parameter. Some of them exhibit a linear variation with temperature while other show an exponential behavior. Finaly, we obtain a nonlinear electrothermal model using 3 controlling variables. The model, is composed of twenty parameters including six temperature dependent. Classical topology and nonlinearities of FET are presented at the figure 3.

Tajima source Ids(V_{gs},V_{ds},T): $I_{dss}(T) = I_{dsso} \times e^{-T/T_{ds}} + I_{dssl}$ $\quad P = P_0 \times T + P_1$

Input diode Igs(V_{gs},V_{ds},T): $I_{s\_gs}(T) = I_{s\_gso} \times e^{T/T_{s\_gs}} + I_{s\_gsl}$ $\quad N_{gs}(T) = N_{gso} \times T + N_{gsl}$

Input diode Igd(V_{gs},V_{ds},T): $I_{s\_gd}(T) = I_{s\_gdo} \times e^{T/T_{s\_gd}} + I_{s\_gdl}$ $\quad N_{gd}(T) = N_{gdo} \times T + N_{gdl}$

An example between the good agreement obtained between measured and modeled ouput characteristics for one of studied temperature T_i is presented in the figure 4. The previous parameters are presented in the figures 9 to 14. As an example, the figure 9 presents the decrease with temperature of the I_{dss} parameter, corresponding to the well known decrease of drain current with temperature. The S-parameters are used to extract and model the nonlinear capacitance behavior.

Thermal resistance determination by pulsed measurement

The second step of the electrothermal characterization concerns the thermal resistance determination to dynamically relate the dissipated power to temperature into the circuit simulator. We are proceding by a non destructive measure of the device whitout any knowledge of the mecanic structure or the parameters of thermal resistivity. The sequence of pulsed used for this measurement is presented at the figure 7. Expressed in °C/W, the thermal resistance gives us the temperature increase above its ambient value following the dissipated power.

$T=T_{ambient}+T_{th}.P_{dissipated}$ where T is the temperature device, $P_{dissipated}= I_{dso}.V_{dso}+ I_{gso}.V_{gso}$

The method is based on pulsed measurement of the input diode characteristic using the threshold voltage Vgs as an electrical thermometer which is very sensitive. This first step consists on a temperature calibration of the input diode characteristic when the dissipated power is set to zero, as it is presented in the figure 5. Thus, for a constant gate current I_g, we can extract the linear curve $V_{gs}=f(T)$ which exhibits a constant slope that lies between -1.2mV/°C and -1.4mV/°C. The second step consists on a dissipated power calibration of the input diode characteristic as it is presented at the figure 6. The transistor is placed at the ambient temperature and we apply a DC quiescent bias to make it dissipate a known DC power P_{DC}. Using pulses, we do not modify the thermal state controled by P_{DC}. Thus, considering the two preceding calibrations for a same gate current sufficienfly high, the cancellation of gate voltage V_{gs} expresses the evolution of the temperature following the dissipated power in the device.

This leads to the definition of temperature versus power characteristic which can be used directly in a nonlinear simulator or to calculate the thermal resistance at a given temperature. The characteristic T=f(P) is presented at the figure 8 and clearly shows the nonlinear nature which can be taken into account according to the needed accuracy of the final model. A first linear approach drives us to a classic constant value of R_{th}, evaluated here at 150°C/W. The nonlinear approach of the curve T=f(P) gives the following modelisation :

$T(P)=T_0(P/P_0)^n+T_1$ where n is real, T_1 is the ambiant temperature, T_0 and P_0 are modeliased parameters

Finaly, it leads to take into account the nonlinear nature of thermal resistance following the dissipated power in the device :

$$R_{th} = \Delta T / \Delta P = R_{tho} \cdot (P)^a \quad \text{where a is real}$$

Results

Measurements and 3D simulations were performed on a power GaAs MESFET with four gate fingers of 0.7µm long and 100µm. The substrate thickness was 100µm and the sources pads were grounded by two via holes. Thermal resitance was found to be 132°C/W by measurement at a dissipated power of 500mW while a value of 125°C/W by the 3D thermal simulation, thus exhibiting a good agreement. The final model has been implemented in the C.A.O. software M.D.S. and presents very good properties of convergence. As an example, the figure 2 shows the good behavior of power added efficiency following the evolution of the source power whtout any optimization.

conclusion

It is necessary to give very care on the thermal performance of active devices. The thermal behavior of power GaAs MESFET was investigated by using both 3D simulation and measurement. A good agreement has been found between simulations and measurements validating the 3D simulation as a predictive tool for the characterization of new power device topologies. Specific Pulsed measurement techniques of S-parameters and I-V characteristics provide an efficient way to characterize electrical and thermal effects. This kind of modelisation represents a real progress for the accuracy

and knownledge of power GaAs MESFET since thermal dependance can be evaluated for a stationary regime. The next stage will concern the measurement of thermal time constant in order to allow dynamic electrothermal simulations. Finaly, this model has been used as a first modeling step in deriving a new electrothermal distributed model well suited to the analysis of the intrinsic operating temperature of each finger.

Acknowledgements:
The authors acknowledge the French D.G.A.-D.R.E.T. for financial support for fruitful discussions on the thermal behavior of the device.

References:

[1] Worhshop on thermal aspects of Microwave device and circuits C.A.D. May 1993, IEEE MTTS
[2] G.Ghione, O.Golzio, C.U.Naldi, « Self consotent thermalmodels of GaAs MESFETs » Alta Frequenza vol.57, n°7, September 1988
[3] P.W.Webb, « Measurement of thermal resistance using electrical method » IEE Proc. Vol.134 Pt.1, ap.87, pp51-56
[4] J.P.Teyssier, M.Campovecchio, R.Sommet, J.Portilla, R.Quéré: « A pulsed S parameters measurement set up fot nonlinear characterization of FETs and Bipolar power transistors », EUMC Digest, Madrid 1993, pp.489, 494.

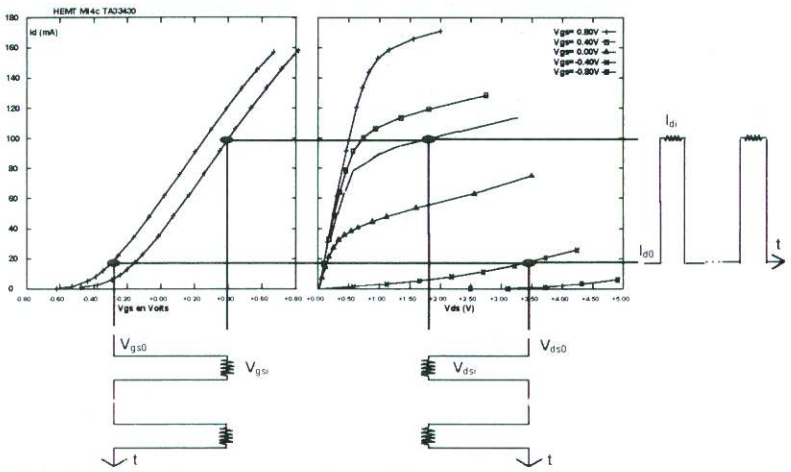


Fig-1 : Schematic representation of the pulsed measurement setup

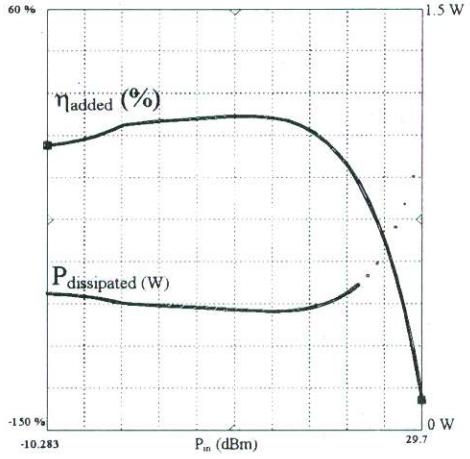


Fig-2: Power added efficiency versus input power

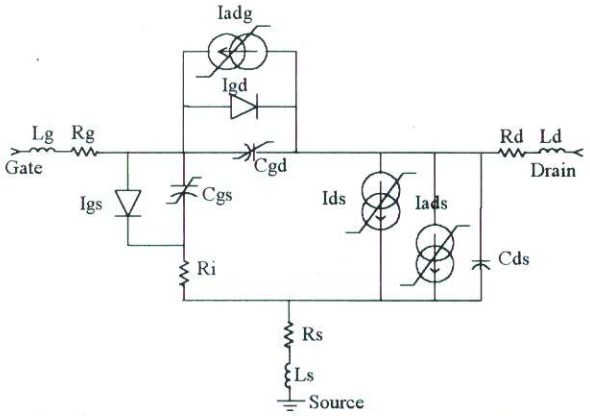


Fig-3 : Nonlinear electrothermal model of the device

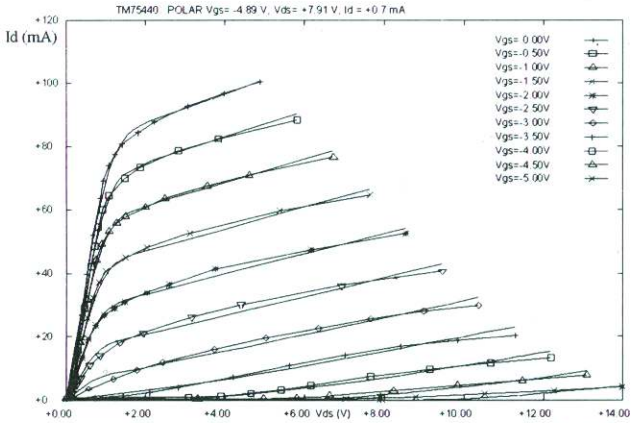


Fig-4 : Drain current characteristic at 23.2°C

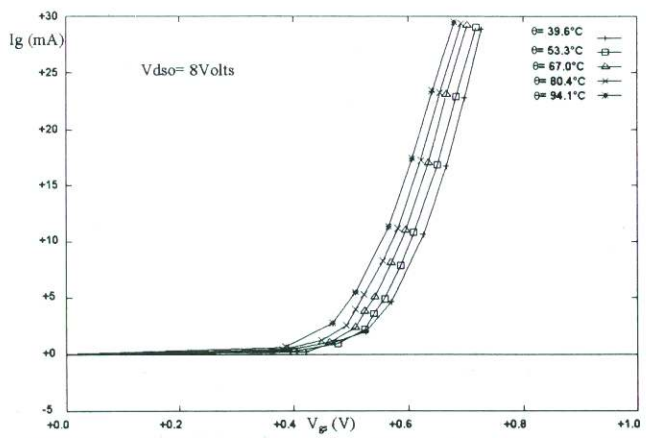


Fig-5 : Temperature dependent gate voltage characteristic

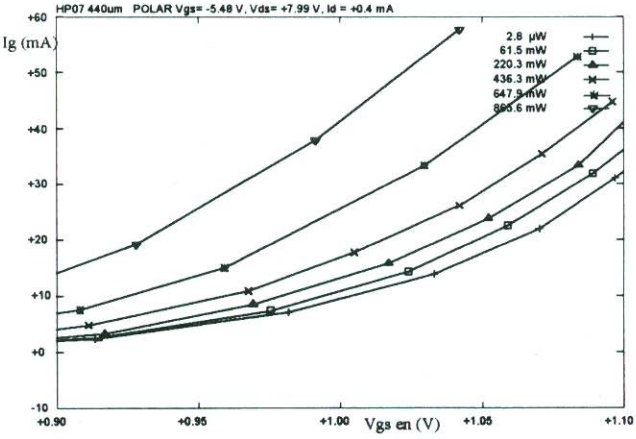


Fig -6 : Power dependent gate voltage characteristic

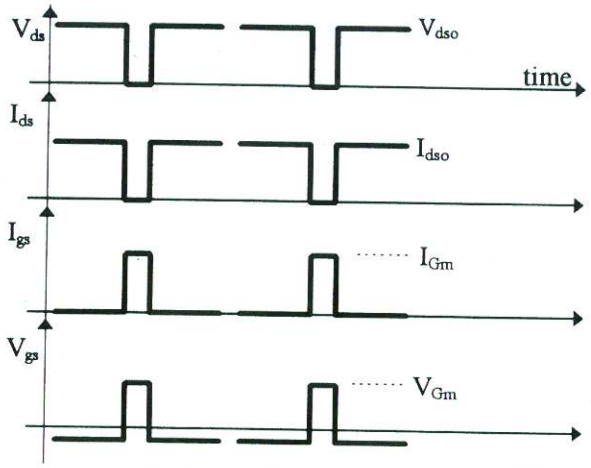


Fig-7 : Sequence of pulses used for the measurement of thermal resistance

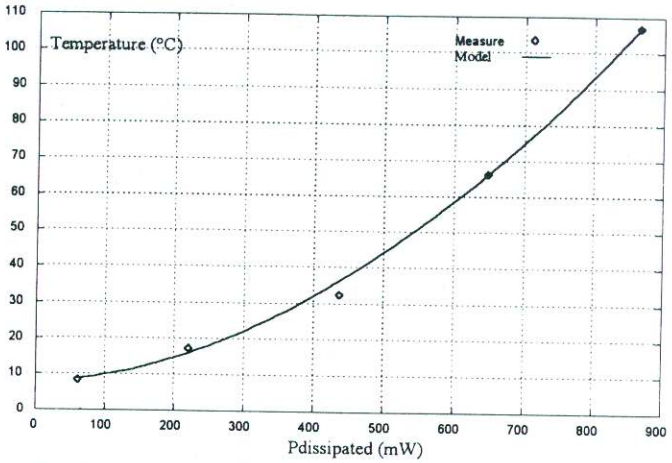
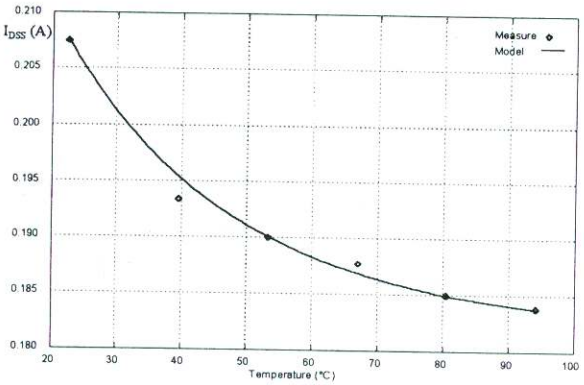


Fig-8 : Variation of the temperature increase versus the dissipated power



I_{dss} versus temperature

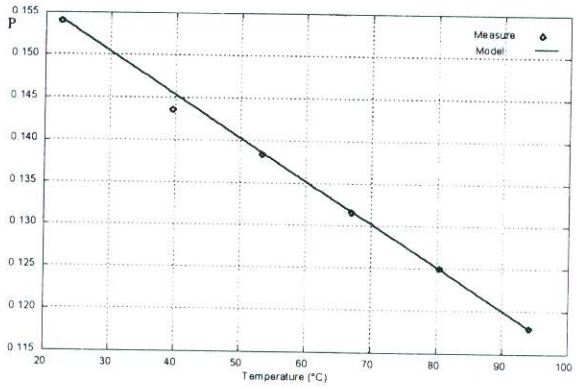
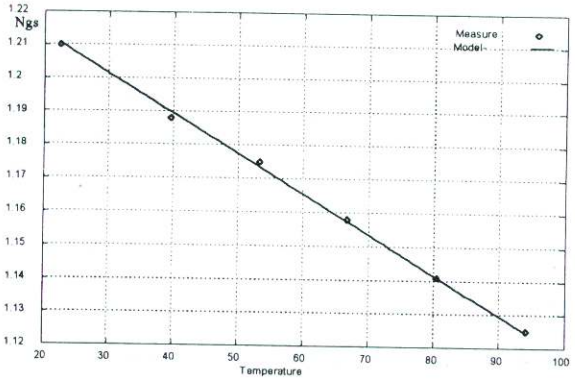


Fig-10 : P versus temperature

Fig-9 :



N_{gs} versus temperature

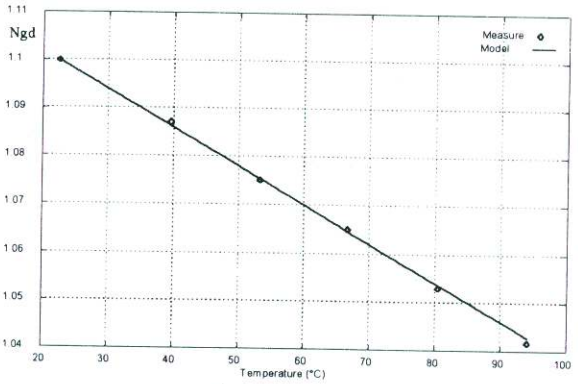
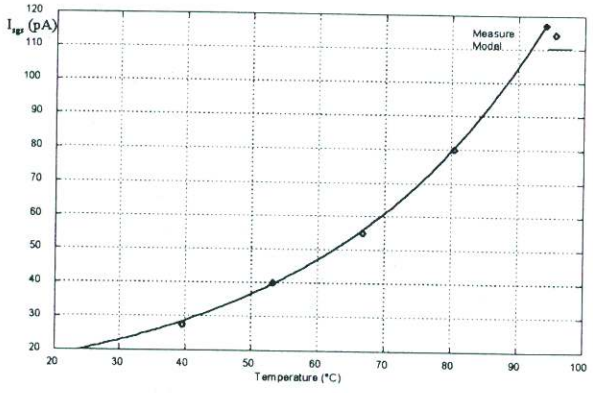


Fig-12 : N_{gd} versus temperature

Fig-11 :



13 : I_{sgs} versus temperature

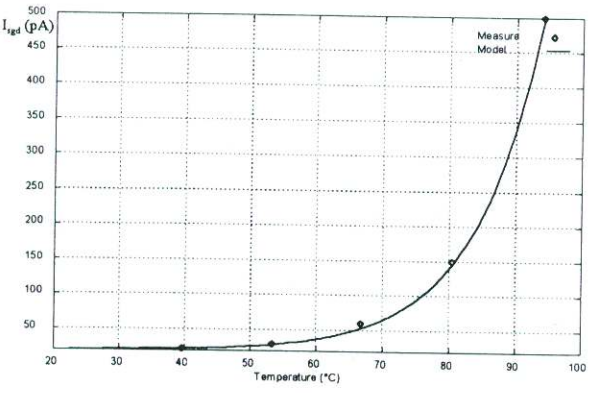


Fig-14 : I_{sgd} versus temperature

Fig-