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Electrical Equivalent Circuit Large-Signal Thermal Modelling for GaAs III-V Devices

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ABSTRACT.- This paper deals with FET's thermal static and dynamic properties for large signal operation. A very simple correction for traditional empirical equations for the Ids current source is proposed. The resulting mathematical approach takes into account the most important characteristics of these devices such as Power efficiency, Low frequency dispersion, Self heating and External temperature dependence. The experimental measurements and electrical modeling approaches has been done for three European foundries using very different topologies and technological process.

I. INTRODUCTION.- The increasing integration of hybrid and monolithic circuits has reinforced the need of accurate large signal models in order to minimize the number of design and fabrication cycles. Therefore it is very important for efficient CAD tools to have good modeling approaches able to predict the small and large signal nonlinear dynamic behavior of GaAs devices when self-heating, dispersion and external heating are present.

Most of the current modeling approaches use DC I/V and multibias Scattering data, along with some dispersion effects, to derive a large signal model. This approach is of questionable validity when dispersion or self heating is important, namely in power devices. In fact each bias point in a GaAs device has their own trap level, surface state ionization and device temperature. That means a different large signal dynamic that obviously cannot be tacked into account by the above approach. Alternative proposed solutions are the use of Pulsed I/V and S measurements at a given bias point, the use of quasi mathematical approaches and/or the use of mathematical table-based models. All of them have their advantages and inconvenients, and for some of them it is not easy to implement into commercially available simulators such as MDS.

This paper pretends the understanding of the different phenomena involved in the nonlinear behavior if the transistor under thermal effects, demonstrating the importance of pulsed measurements and the influence of the quiescent operating point on this dynamic. This approach will be developed in terms of an easy implementation into commercially available simulators and will be verified by measurements performed on very different transistor sizes and technologies.

II. LARGE SIGNAL DYNAMIC MODEL.- The importance of nonlinear characterization of transistors form equithermal pulsed measurements have been demonstrated by several authors [1-4]. Thermal effects caused by self-heating change the internal parameters such as electron mobility, ionisation breakdown or schottky barrier characteristics. Low frequency dispersion, mainly in the transconductance and output conductance, has been associated with deep traps and surface states in GaAs devices and greatly affects the dynamic of the transistor. Both effects, obviously, cannot always be easily separed in an electrical equivalent circuit model.

Since it is no easy to separate these two effects, we can choose an appropriate analytical equation for the I_{ds} current source:

$$I_{ds}(t) = FNL(V_{gi}(t), V_{di}(t), V_{gio}, V_{dio}) \qquad (1)$$

where the dependencies on the instantaneous control voltages, $V_{gi}(t)$ and $V_{di}(t)$, and the static part, V_{gio} and V_{dio} are introduced. If we want to take into account the cut-off frequency that controls the transition between DC and RF, we must consider two current sources: the first one for the purely static DC characteristics and another one in series with capacitor [3] that corrects the dispersion and internal self-heating:

$$I_{ds}(t) = FNL1(V_{gi}, V_{di}) + FNL2(V_{gi}, V_{di}, V_{gio}, V_{dio}) \qquad (2)$$

As equation (2) must reproduce any dynamic from any bias point, it seems evident that it should be necessary to measure the pulsed I/V curves at a large amount of quiescent bias points, although our experience [xx] says that there are a few key points that are enough to derive the mathematical equation.

Furthermore, this I_{ds} equation, as well as most of linear and nonlinear elements in the equivalent circuit, must be modulated by the transistor gate geometry **W**:

$$I_{ds}(t) = FNL1(V_{gi}, V_{di}, W) + FNL2(V_{gi}, V_{di}, V_{gio}, V_{dio}, W) \qquad (3)$$

Finally the breakdown effect must be measured under pulsed condition for different quiescent operating points because the static DC breakdown always occurs at lower drain voltages than in RF conditions.

III.CORRECTION FOR EXTERNAL TEMPERATURE.- Adding the external temperature dependence, **T**, to equation (3), we can obtain a general model taking into account the internal scaleable self-heating of the transistor due to the internal dissipated power as well as the low frequency dispersion. This new equation is shown in (4).

$$I_{ds}(t) = FNL1(V_{gi}, V_{di}, W, T) + FNL2(V_{gi}, V_{di}, V_{gio}, V_{dio}, W, T) \qquad (4)$$

To carry out this modelling way, we have to accomplish the coupling of the Network Analyzer and the Pulsing System to a thermal chamber, so we can perform the needed measurements in a wide range of plate temperature.

Under DC behaviour, it is clear that the main thermal dependence appears for the saturation current and Pinch-off voltage parameters. Fig.1 and Fig.2 show the thermal DC dependence of the Drain current source for the two extreme conditions. It seems evident that it is very easy to find appropiate expressions for this dependence and consequently to embeed into nonlinear simulators.

However, in the case of the Dynamic thermal behaviour the aspect of the phenomena is very different. It can be observed that not only absolute levels but also the slopes are different depending on the external temperature and the internal dissipated DC power (quiescent operating point). Fig. 3 shows this dependence for the $\mathbf{I_{dss}}$ and $\mathbf{V_{TO}}$ parameters for a 10*140 μm GEC-Marconi device.

In order to validate the proposed electrical model, many simulations have been done. As an example, Fig.4 shows comparison between simulations and measured data under Pulsed I/V operation for a 10*140 μm GEC-Marconi device with 261°K at (-1'5,3) bias point. A very good agreement between simulations and experimental data can be observed.

IV. CONCLUSIONS. A new modelling way for group III-V GaAs devices has been presented. This modelling allows us to obtain a general expression for the $\mathbf{I_{ds}}$ current source taking into account the well know second order effects [6] as well as the external temperature dependence of this current. Comparisons between simulations using this model and experimental result, demonstrate the validity of this approximation.

REFERENCES

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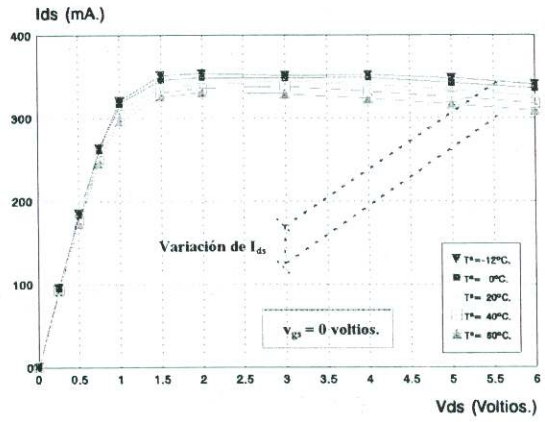

Fig. 1: DC Thermal Variation for V_{gs} = 0 volt.

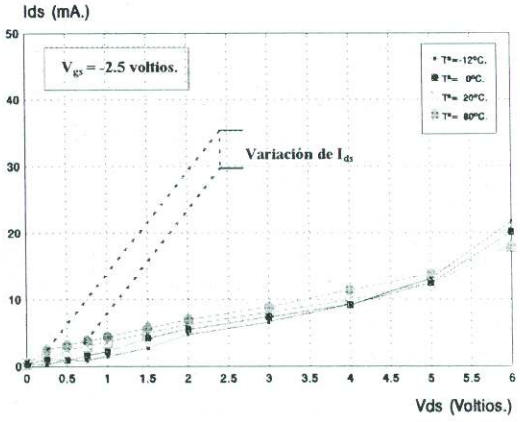

Fig. 2: DC Thermal Variation for V_{gs} = -2.5 volt

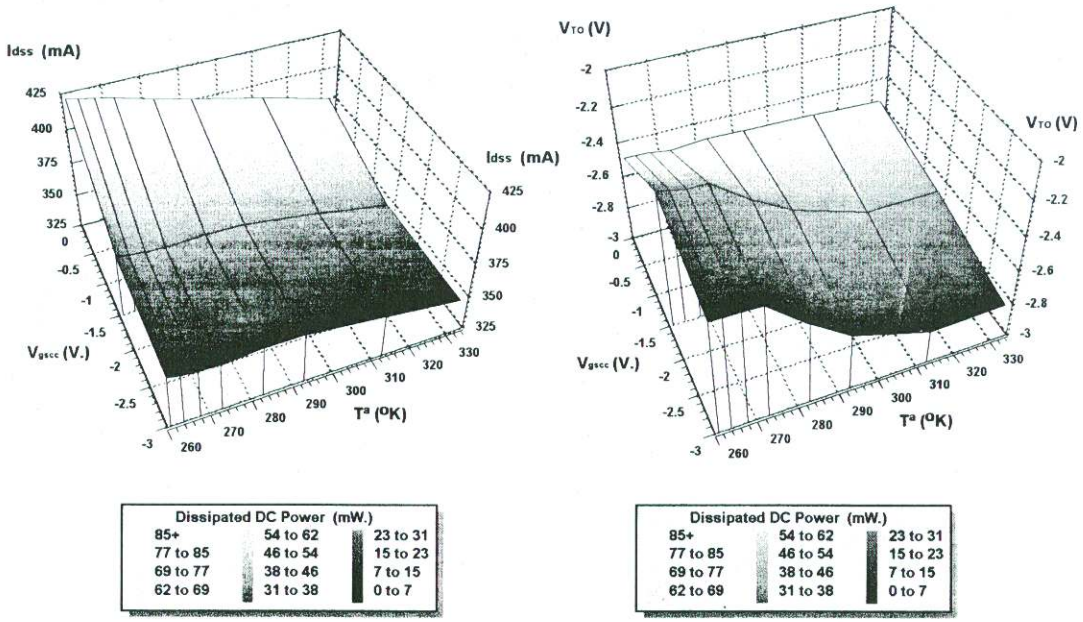

Fig.3.- Idss and Vto Thermal Variation

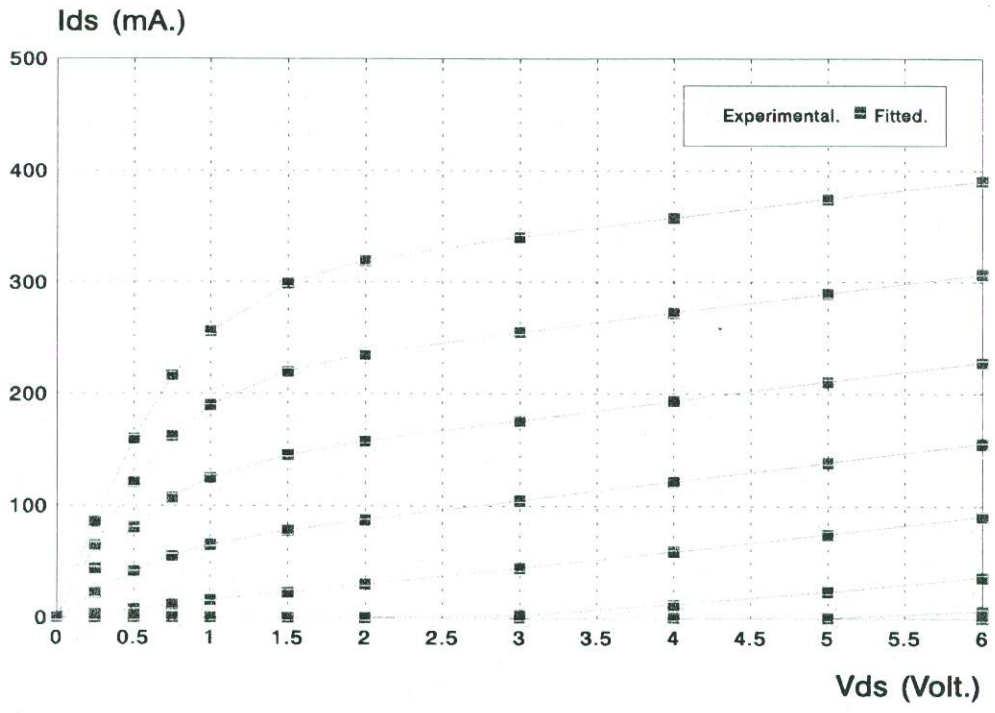

Fig.4.- Experimental vs. Simulated Thermal Dynamic