GAAS® 97 • 5th European Gallium Arsenide and related III-V compounds Applications Symposium
Bologna, Italy - September 3rd-5th, 1997

SCALABLE DISTRIBUTED MODEL FOR MICROWAVE AND MILLIMETRE-WAVE MONOLITHIC FET-TYPE DEVICES

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ABSTRACT

In this contribution, the authors report an approach for constructing a scalable small-signal distributed model. This model, whose elements are defined per unit gate width, has been used to simulate the small-signal behaviour of three monolithic MESFET devices which only differ in the gate width (25, 50 and 75 μm). S-parameters measured in the 1-40 GHz frequency range at a wide variety of bias conditions were used to perform the simulations. The difficulty to produce good scalable models is shown as well as the need to make use of measurements of identical devices with different gate widths, not only to develop a scalable model, but also to provide physical meaning to the equivalent circuit.

INTRODUCTION

For efficient monolithic circuit design, device models which provide good accuracy and can be scaled with the physical dimensions of the components are needed. Scalable models are those where the values of each equivalent circuit element are defined per unit length. This characteristic is especially useful to assess the performance of FET type devices by modifying its gate width, and also helps in understanding the device physics. Also, the distributed nature of this type of devices, as well as its influence both in the parameter extraction technique and in the simulation of the small-signal characteristics of the device, make it necessary to take into account the distributed effects in the scaling procedure.

In this contribution, a scalable distributed model especially designed for monolithic circuit applications is used [1]. The intrinsic device model takes into account the transverse propagation along the electrodes and is characterised by two matrices defined per unit gate width. Scaling rules are straightforward in this kind of model and the use of heuristic scaling rules is therefore avoided. The distributed model was used to simulate the small-signal behaviour of three monolithic MESFET devices which only differ in the gate width (25, 50 and 75 μm). The topology of the intrinsic model is the result of the simulation of the cold-FET by using a simplified lumped element equivalent circuit. Important conclusions about the physical origin of the elements of the model are therefore reached. The fact that the distributed nature of the device has a very important role and that it must be considered in order to explain the behaviour observed in the elements of the model is also shown.

SCALABLE LUMPED ELEMENT MODELS

Several models for FET devices intended to be scalable and based on layout structures and gate width have been used [2,3]. In most cases they are lumped element models in which the scaling of the elements obey complicated heuristic rules which are empirically determined based on experience, and are far from intuitive. This is the main reason why so many scaling rules definitions are found, especially when it comes to extrinsic elements. Many authors have even proposed scaling rules for these elements that, although improve the simulation of the small-signal characteristics of the device, lose the physical meaning of the model [2,4].

In order to discuss the limitations of scalable lumped element models a classical one [5] has been used to simulate the measured S-parameters of the three devices. Fig.1 shows the gate inductance (L_g) versus V_{gs}, with the gate width as a parameter, under zero drain bias conditions. The figure clearly shows that L_g is not independent of the gate width and bias conditions. This may explain why bias dependent and gate width scaled extrinsic elements have been used to improve the simulation performance [2]. A good fitting of the S-parameters can be achieved using this approach, but the physical background of the model is lost. In fact, this leads to model parasitic elements dependent on the active device structure, even though they clearly must be external to the structure. A good model should not need to have extrinsic elements scalable.

The behaviour observed in extrinsic elements when using a lumped element model is due to propagation effects, and can only be properly interpreted by using a distributed model [6]. This effect becomes more important as the gate width increases.

If the device dimensions are of the same order of magnitude as the wavelength, lumped element approximation is no longer valid and distributed properties must be included. The limits of the lumped element approximation do not only depend on the frequency but also on the physical size of the device. Consequently to develop a fully scalable physically related model the distributed nature of the device can not be ignored.

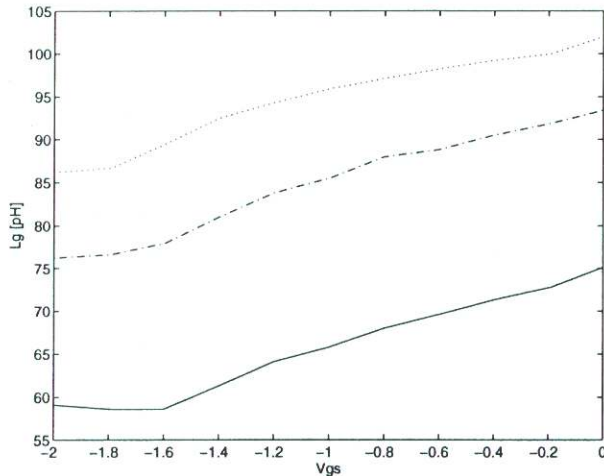

Fig. 1 Extrinsic gate inductance versus gate voltage for V_{ds}=0 (—25 mm, - -50 mm, ····75 mm)

SCALABLE MODEL DEVELOPMENT

The first step in constructing a scalable model is to define the right topology for the equivalent circuit capable of describing the behaviour of the active device. It is clear that a physically related topology is needed for scaling purposes, and also measurements of various devices with different gate widths are needed in order to be able to identify the location of the elements of the model. In fact, the use of measurements of devices with different gate widths can provide a deeper insight into the physical origin of the elements of the intrinsic model and allows series and parallel effects to be differentiated. The distinction between both contributions can be carried out by studying the dependence of the elements of the model with the gate width. In addition, parasitic effects must be separated by using residual values of elements linearly dependent on the gate with. This technique can provide a reliable and robust determination of extrinsic elements.

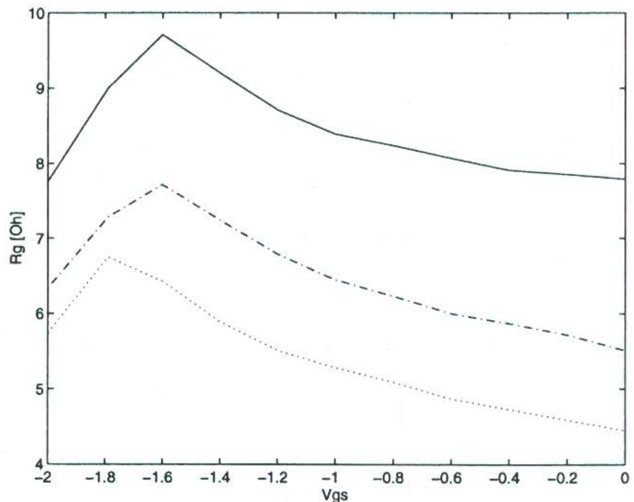

Fig. 2 Extrinsic gate resistance versus gate voltage for V_{ds}=0 (—25 μm, - -50 μm, ····75 μm)

The results obtained from the simulation of the cold-FET by using a simplified lumped element model are examined. One interesting result is shown in Fig.2, where the value of the total gate resistance of a classical lumped element model for the three devices under zero drain bias conditions is plotted. It can be observed that the total gate series resistance depends on both the bias conditions and the gate width. This resistance can be divided into three parts: one constant (the parasitic resistance, R_g), one proportional to the gate width (related to propagation effects, R_{tg}), and one inversely proportional to the gate width (R_i and R_f). It transpires from Fig. 2. that R_i and R_f are in this case the dominant part of the total gate series resistance for short gate widths, and R_g will hence be overestimated if R_i and R_f are not taken into account. Notice that these three components of the gate resistance can only be properly identified if measurements of devices with different gate widths are available.

The dependence with the gate width of the remaining elements of the lumped model have also been analysed. Parasitic elements have been extracted and an equivalent circuit topology, suitable to simulate the intrinsic device, has been obtained.

SCALABLE DISTRIBUTED MODEL

To overcome the limitations of the lumped model the use of a distributed model [1] is proposed. This model takes into account the propagation along the device width, and has been deduced from the analysis of the

FET structure, which is considered to be a non-symmetrical non-reciprocal coupled line system in a non-homogeneous medium. The main hypothesis is to assume that the FET can be characterised by two matrices, the impedance matrix and the admittance matrix, defined per unit gate width (Fig.3). The topology of the admittance matrix is that derived from the previous analysis with the conventional lumped element model.

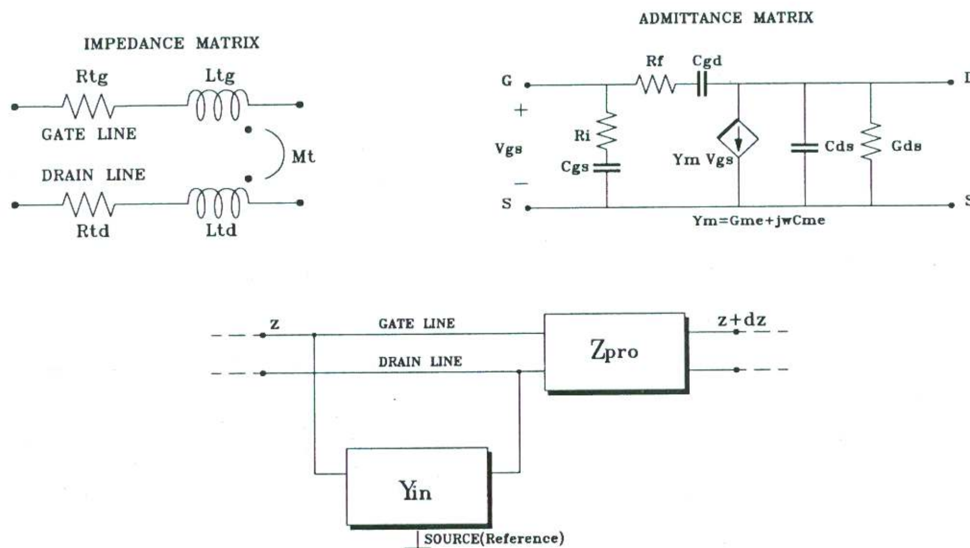

Fig. 3 Equivalent circuit per unit gate width of the distributed model

The simulation of the three MESFET devices by using the distributed model was performed in two different ways: (i) carrying out the optimization for each device individually and (ii) collectively. Firstly, each device was simulated one by one without making use of the information from the other almost identical devices available. The optimization process was performed fitting the measured S-parameter data of a single device. The results obtained in this first phase prove that the chosen equivalent circuit topology is the most appropriate, and that the elements follow the scaling rules. The model provides an excellent fitting of the small-signal characteristics of the device over all operating bias points. Secondly, the three MESFETs were simulated simultaneously, forcing the fulfilment of the scaling rules in the optimization process, that is, the optimization process was performed using the S-parameter data of the three devices of different sizes. The results which were obtained in this way are very similar to those of the previous phase, which again confirm the validity of the model. Moreover, the process is very reliable and robust because initial parameter values of the optimization process hardly have any influence on it.

The error of the individually optimized model is lower than that of the scalable model. There is a trade-off between model accuracy and scalability because in this situation the benefits offered by the scaling are achieved at the expense of accuracy. This drawback can be overcome by including the "effective gate width" as a new parameter in the optimization process. This new parameter is added to account for devices not being exactly identical as far as their transversal section is concerned. The results obtained for the effective gate width are almost independent of the bias conditions, which again supports the validity of this approach.

The bias dependence of some elements of the admittance matrix of the equivalent circuit, for the three MESFETs, is displayed in Fig.4. Results both from the individual simulation and from the collective simulation are shown. These curves corroborate the consistence of the proposed model.

The obtained results question the parameter extraction methods based on using lumped element equivalent circuits. These methods, which ignore transverse propagation effects in the device, can lead to erroneous values for the elements of the model. Therefore, the distributed nature of the intrinsic device has to be taken into consideration if a proper extraction of the elements values or a fully scalable model is required.

CONCLUSIONS

Limitations of scalable lumped element models have been discussed. The deviations from the scale law when using lumped-element equivalent circuits can be explained by using a distributed model. The obtained results reveal the need to make use of measurements of identical devices with different gate widths in order

to develop device models with physical meaning. The distributed nature of the device must be taken into account through the use of a distributed model for accurate and consistent modelling of this kind of devices.

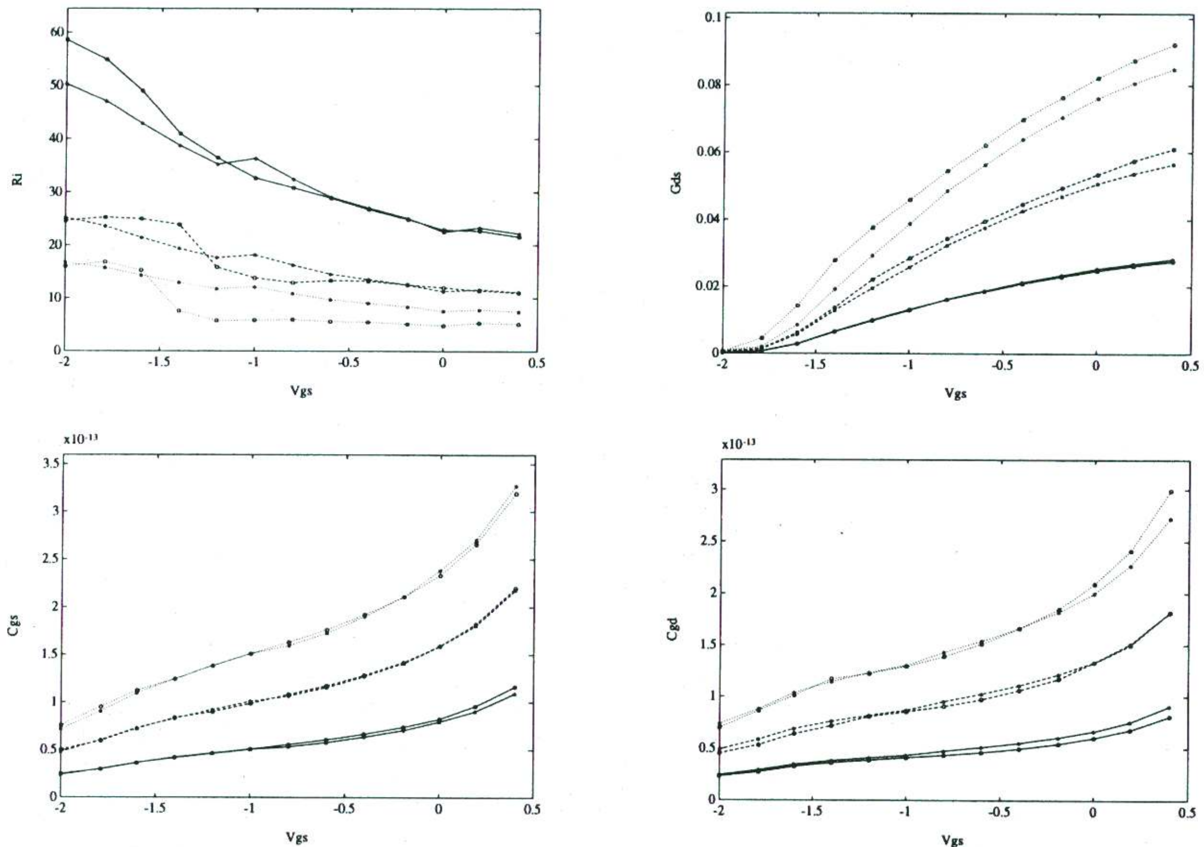

Fig.4. Admittance matrix elements as a function of V_{gs} for V_{ds} =0 and with the gate width as a parameter. (Individual optimization: —o—25 μm,–o–50 μm, ·· o ··75 μm; collective optimization: —*—25 μm,–*–50 μm, ·· * ··75 μm)

An extraction approach for determining a scalable distributed small-signal model of FET-type devices which is physically meaningful has been described. This model has been applied to three MESFETs of different sizes. The optimization procedure was performed individually for each device and then collectively. The former operation produced a set of model parameters which almost follow the scaling rules. The latter produced a set of parameters which exactly obeyed the scaling rules. The results are shown to be accurate up to 40 GHz, even when the parameters of the model are forced to obey the scaling rules.

ACKNOWLEDGMENT

The authors would like to thank Prof. G. Leuzzi (University of Roma "Tor Vergata") for providing the experimental measurements used in this study. Financial support under grant TIC95-0843 by the spanish "Comisión Interministerial de Ciencia y Tecnología" is gratefully acknowledged.

REFERENCES

[1] C. Camacho Peñalosa, T.M. Martín Guerrero, B. Castillo Vázquez, "Distributed Modelling of Microwave and Millimetre-wave FETs", to be presented at *ISRAMT*, Beijing (China), August 1997.

[2] J. Rodríguez Téllez, K.A. Mezher, "Effect of Scalability on Nonlinear MESFET Model Accuracy", *Proc. of the 24th European Conference,* pp. 1632-1637, Cannes (France), September 1994.

[3] J.M. Golio, 'Microwave MESFETs & HEMTS', Artech House, 1991.

[4] S.W. Chen, O. Aina, W. Li, L. Phelps, T. Lee, "An Accurately Scaled Small-Signal Model for Interdigitated Power P-HEMT up to 50 GHz", *IEEE Transactions on Microwave Theory and Techniques*, **vol. 45**, no. 5, May 1997.

[5] G.D. Vendelin, M. Omori, "Circuit Model for the GaAs MESFET valid up to 12 GHz", *Electronic Letters*, **vol. 11**, pp. 60-61, 1975.

[6] T.M. Martín Guerrero, B. Castillo Vázquez, C. Camacho Peñalosa, "Identification of HEMT nonlinearities by using an intrinsic distributed model", *Proceedings of the 4th International Workshop on Integrated Nonlinear Microwave and Millimetrewave Circuits*, pp. 89-94, Duisburg (Germany), October 1996.