Mixed Signal High Integration MMIC Phase Control Device for Application in Phased-Arrays

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A MMIC multi-port highly-integrated phase control device, suitable for application in low cost phased-array antennas is presented. The MMIC consists of eight LNAs, eight sets of RF-switches, a phase manifold, eight phase shifter networks for phase control and two 4 to 1 output power combiners. The DC power supply circuitry, the digital control circuitry and the RF sub modules are combined on the same die. The chip is designed in a mixed analog / digital 0.25 μm PHEMT technology. It is shown that the functionality of this chip is equivalent to eight separate 3-bit phase shifters.

INTRODUCTION

The large number of phase shifters that are necessary for the realisation of phased array antennas set the requirement for highly integrated and low cost MMICs. This paper emphasizes on a low cost phase control device (PCD) using a patented architecture – Shem-Tov Levi (1). The PCD is developed as MMIC and is implemented in a limited scanning phased array antenna as described in Toshev et al (2).

MMIC ARCHITECTURE AND PRINCIPLE OF OPERATION

The block diagram of the MMIC is shown on Figure. 1. Eight input RF signals arrive at the inputs of the patch selectors (PS1-PS8) after amplification by 8 identical LNA's. The patch selector itself is a set of switches and allows its input to be connected to each one of its eight outputs. By means of the patch selectors and the phase manifold it is possible to route each of the input signals through one of the fixed phase shifters (Φ1-Φ4). If two or more input signals have approximately equal phases they are first grouped in the manifold combiners (MC1-MC8) as shown on Figure. 2 and then passed through a common fixed phase shifters. In this way a dynamic grouping of the input signals is implemented depending on the phase state of the PCD. The patch selectors control the dynamic grouping. The equivalent RF scheme of the PCD for two different states is shown on Figure. 2. There are two equal sets of fixed phase shifters – each containing shifts between 0° and 135° with 45°

steps. Signals from each set are combined in the corresponding output power combiner, resulting in two RF outputs. The MMIC can be used as the equivalent of eight 3-bit phase shifters if an external 180° phase shift is applied at one of the RF outputs and then its signal is combined with the second MMIC's output.

MMIC DESIGN AND LOW COST PACKAGING

LNA Design

A two-stage LNA has been designed. A gain of more than 18.5 dB and a noise figure below 1.7 dB over the band of interest is simulated. The input and output impedances are 50 Ω. The 1 dB compression point is more than 2 dBm. Eight LNAs are integrated on the chip and are situated in pairs at the four die's corners. Except for the input matching circuits, the designs are kept symmetrical to ensure equal amplitude and phase responses; the ground planes separating the LNAs minimize the mutual RF-coupling.

Patch Selectors

Eight patch selectors are integrated on the chip. Each patch selector has one input connected to the LNA output and eight outputs connected to the patented phase matrix (manifold). The patch selector is built from 8 dual gate FETs and a 1 to 8 distributed feed network. This distributed network is designed to have minimum phase differences between the signals at the output of the patch selectors.

Phase Manifold

The phase manifold is the heart of the chip. It is passive and its aim is to connect the outputs of the patch selectors to the phase shifters in every possible way. The phase manifold has 64 RF input lines and 8 RF output lines. To minimise the coupling between the signal lines, ground planes are placed in-between.

Phase Shifters

Eight fixed phase shifters have been designed. The differential phase shift between them is in the range of 0° and 135°, distributed equidistantly. All phase shifters are composed of passive high-pass networks for phase shifting and input low-pass networks for matching. Lumped planar elements were used for this purpose.

Power Combiners

Two equal phase power combiners each having four inputs and one output have been designed in a way that provides switching, combining, impedance matching, odd-mode rejection and loading of branches that are not connected to the output. The input impedance of the combiner is 25Ω and the output impedance is 50 Ω.

Digital Driving Circuitry

A 72-bit shift register and the additional I/O control circuit are integrated on the chip. To obtain the required functionality each shift register bit comprises of 3 D flip-flops and a FET-driver, while the I/O control block contains clock pulse generator, TTL/DCFL converter and DCFL/TTL converter. The digital transistors have two threshold voltages – enhanced and depleted mode and the GaAs logic is direct-coupled FET logic (DCFL).

MMIC Packaging

A low-cost leadless chip carrier on TMM10i organic substrate is designed and manufactured. The lid cover is of plastic and is glued on the top surface of the carrier. I/O castellation and via transitions are used. Grounded coplanar wave guide (GCWG) transmission lines and internal matching circuits are used in order to decrease the multi-port coupling and to compensate for the bond wire reactance's. The bare die is attached by silver-filled epoxy. Gold wire bonds are used for the RF connections from the carrier to the die. The metal surface of the carrier is gold plated.

TECHNOLOGY IMPLEMENTATION OF OMMIC

The ED02AH 0.25 μm PHEMT technology of OMMIC was used for the chip production. This process gives the opportunity to combine RF functions and digital control circuitry on the same die. The unique combination of normally ON (depleted mode) having a low threshold voltage and normally OFF (enhanced mode) transistors having a high threshold voltage makes it possible to design DCFL digital circuits with a low power dissipation.

MEASUREMENTS RESULTS

The MMIC patented principles of operations as well as its architecture are property of Sky Gate. The layout and electrical design of the MMIC was performed by TNO-FEL in the Netherlands. A photograph of the MMIC and a photograph of the MMIC on the carrier are shown on Figures 3a and 3b respectively.

Two types of tests were performed with the MMICs. On wafer RF and digital measurements were performed at TNO-FEL with the objective to validate equality of the chip parameters with respect to position on the wafer.

Measurements of the MMICs on the carriers were performed at a later stage at Sky Gate BG to validate the overall performance of the MMICs including the package. Table 1 summarizes the most important RF and system level parameters. The measured results of the insertion gain and insertion phase, when signal is passed through different fixed phase shifters, are shown on Figure 4a and 4b respectively. It can be observed that the amplitudes for all branches are identical and that the phase shifts between signals have been accomplished.

DISCUSSION AND CONCLUSION

To make the chip attractive for commercial applications, its size and DC-power consumption have been minimized to every extend. The overall power consumption is 920 mW. An innovative phase routing and combining matrix circuitry for RF signals is demonstrated. RF sub-modules and digital driving circuitry are integrated on one die. Electromagnetic simulators have been used extensively in order to predict the RF coupling between signal lines and to reduce it to the minimum. A low-cost package with excellent RF performance is designed and fabricated.

The use of innovative and highly integrated structures resulted in a small MMIC with a low power consumption considering its functionality.

REFERENCES

(1)   Shem-Tov Levi, European patent no. 0916168 – *"A Phase Control Device"*

(2)   A. Toshev, E. Totomanov, M. Gatchev, B. Marinov, I. Stoyanov, S. Kamenopolsky, *" Flat Limited Scanning Phased Array Antenna for DBS Reception"*, paper sent to 32 European Microwave Conference 2002, September 23-27, 2002, Milan, Italy

Table 1
MMIC RF and system level parameters

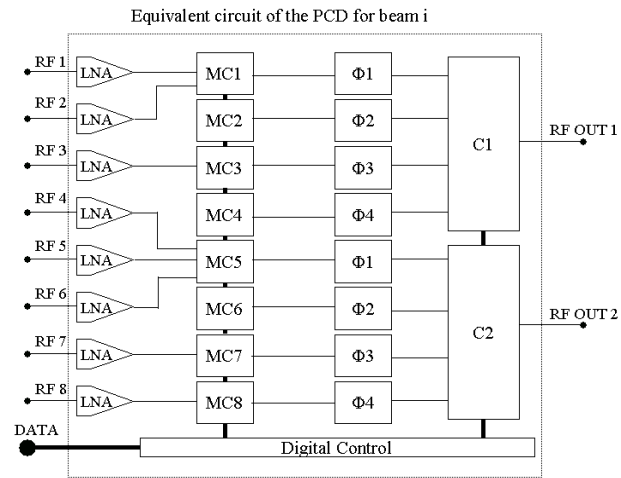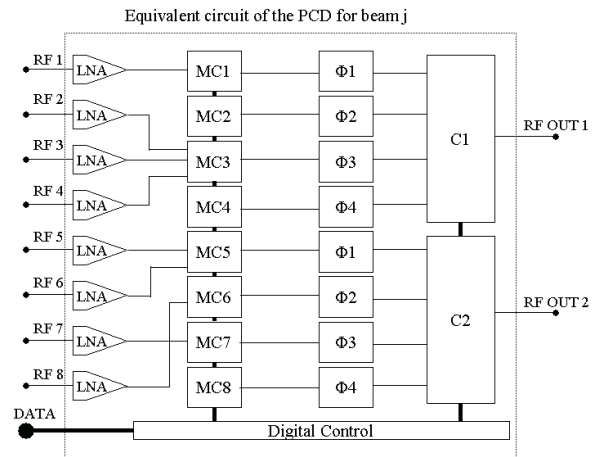| Measurements with carrier	On wafer measurements
• Input reflection (VSWR) – below 1.9 • Output reflection (VSWR) – below 2.6 • Noise Figure – average 5 dB • Insertion gain – average 6 dB • Port to port isolation – below –20 dB • Power consumption – 1W	• Input reflection (VSWR) – 1.23 … 1.67 • Output reflection (VSWR) – 1.18 … 2.1 • Noise Figure – average 3.5 dB • Insertion gain – average 6.5 dB

PS1÷PS8 – Patch selectors; Φ1÷Φ4 – Fixed phase shifts; C1, C2 – Output power combiners
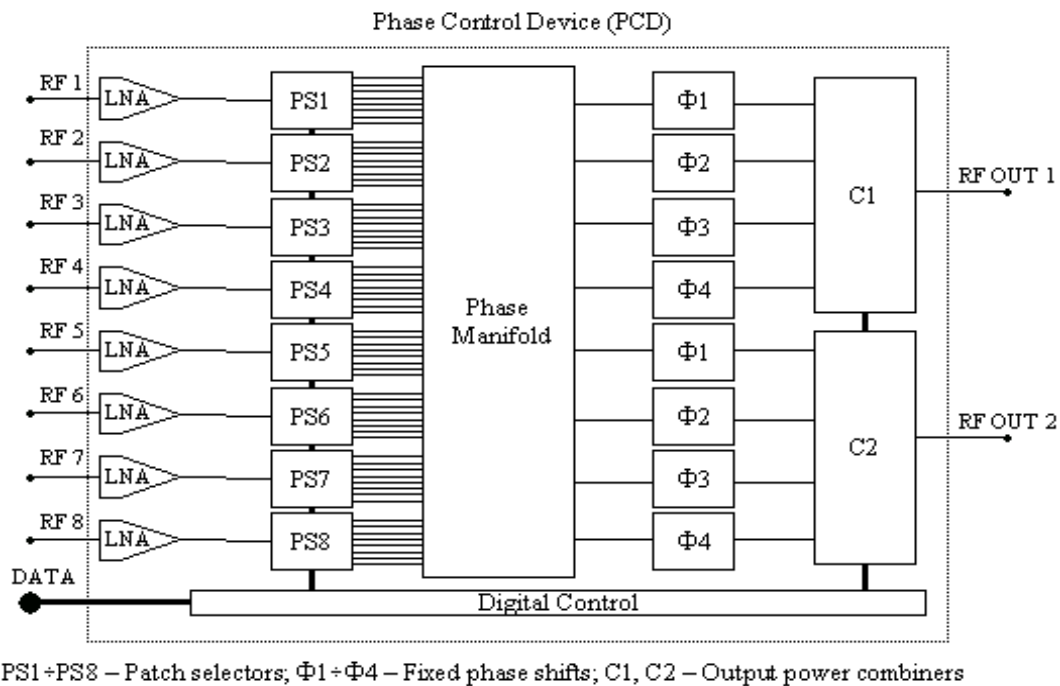
Figure. 1.Block diagram of the MMIC

Equivalent circuit of the PCD for beam i

MC1÷MC8 – Manifold combiners; Φ1÷Φ4 – Fixed phase shifts;

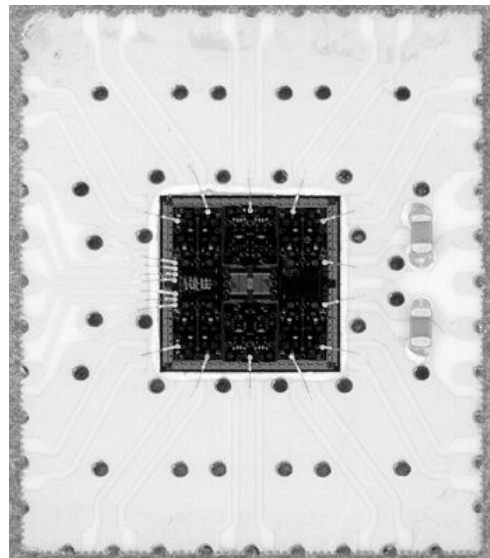C1, C2 – Output power combiners

Equivalent circuit of the PCD for beam j

MC1÷MC8 – Manifold combiners; Φ1÷Φ4 – Fixed phase shifts;

C1, C2 – Output power combiners

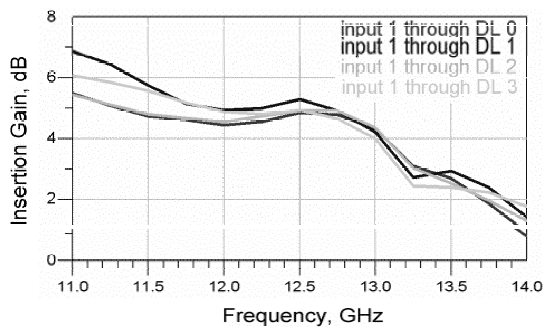Figure 2. Equivalent RF scheme of the PCD for two different beams
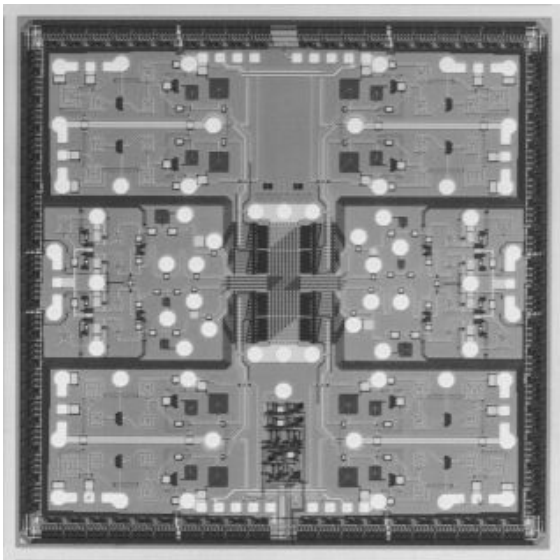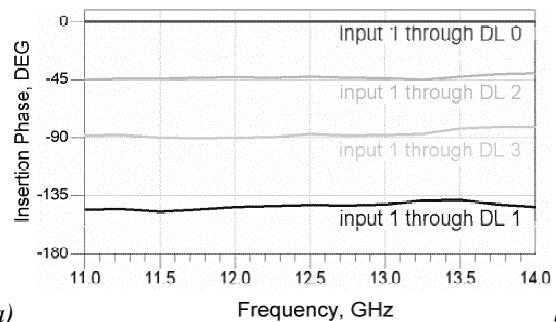

(a)

(b)

Figure 3a: Picture of the bonded MMIC

3b: Picture of the MMIC and carrier

a)

b)

Figure 4a: Measured insertion gain of the MMIC with carrier

4b: Measured insertion phase of the MMIC with carrier