Power RF-Operation of AlGaN/GaN HEMTs Grown on Insulating Silicon Carbide Substrates

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Abstract

We report on the technology and microwave characterization of AlGaN/GaN power HEMTs on SiC substrate. DC and S-parameter are discussed, together with load-pull results on devices up to 4mm gate width. A power density of 5.2 W/mm is obtained for devices up to 2 mm gate width. The maximum power level achieved is 13.8 W at 2 GHz.

INTRODUCTION

Due to their high breakdown field and excellent electron transport properties AlGaN/GaN HEMTs offer several advantages for high power microwave applications. These advantages include high operation voltage, high output impedance and high cut-off frequency. Furthermore, SiC as a substrate material provides an excellent thermal conductivity, comparable to copper which is mandatory for effective heat removal in high power applications. These features account for the capability of power combining up to very high absolute microwave output power levels. The introduction of these devices for system level GaN based power amplifiers and MMICs requires reproducible processing techniques established on state-of-the-art process lines. Lossy et al (1). This paper is intended to support this notion.

EPITAXY

The $Al_{0.25}Ga_{0.75}N$ /GaN HFET structures were grown by MOCVD on SiC 2"-wafers. The epitaxial growth structure starts with the deposition of a 500 nm thick AlGaN layer followed by a 2.7 µm GaN buffer layer, 3 nm $Al_{0.25}Ga_{0.75}N$ spacer, 12 nm Si-doped $Al_{0.25}Ga_{0.75}N$ supply layer, 10 nm $Al_{0.25}Ga_{0.75}N$ barrier layer and a 5 nm thick GaN cap layer. Hall data from samples grown on n-SiC exhibit $n_{2DEG} = 7.8\times10^{12}$ cm^{-2}, $\mu_n = 1400$ cm^2/Vs at RT.

TECHNOLOGY

Device fabrication was accomplished using 0.5 µm stepper lithography. Source and drain ohmic contacts have a metallization consisting of Ti/Al/Ti/Au/WSiN (10/50/25/30/120 nm) with improved edge and surface morphology. Due to the properties of the WSiN sputter deposition process the Ti/Al/Ti/Au-layers, which are deposited by e-beam evaporation, are totally embedded. While standard ohmic source and drain contacts without WSiN are very rough after rapid thermal annealing at 850° C, both the surface and the contours of the metallization employed here are still smooth and well-defined after annealing.

CONTACTS

The contact resistance is analysed by TLM measurements with respect to thickness and composition of the different metallization layers at different temperatures. Results show that our metallization scheme is optimum at low doping concentration. The contact resistance is determined to be 0.5 Ωmm under these conditions. We find the ohmic contact covered by WSiN to be stable in electrical performance and morphology for temperatures of 400°C up to 120 hours. Lossy et al (2). The uniformity of sheet resistance and contact resistance determined by TLM is rather good, resulting in a standard deviation below 3 % for these quantities.

Table 1: Contact resistance R_C (Ωmm) for different metal elements and thicknesses at different RTP temperatures.

Metal nm	RTP 830°C	RTP 800°C
Ti Al Ti Au 10 100 20 50	1.176 ±0.196	2.78
Ti Al Ti Au 10 50 20 50	0.542 ±0.069	0.65 ±0.066
Ti Al Ni Au 10 100 20 50	1.516 ±0.187	2.5
Ti Al Ni Au 10 50 20 50	1.195 ±0.517	3

Gate contacts are made from a Pt/Au metallization and a gate length of 0.5µm is obtained using stepper lithography. Additionally, devices with L_G=0.28µm are written using a shaped electron beam tool (ZBA23-40kV). Large devices with different gatewidths ranging up to 4 mm were fabricated using an airbridge technology .

DC-CHARACTERISTICS

Measurements reveal a saturated drain current of I_{DSS}=1.2A/mm (V_G=+2V). Due to the excellent contact resistance (0.4….0.6 Ωmm) the normalized source-gate resistance is generally 0.85-0.9 Ωmm. From this the intrinsic $g_{m,max}$ is calculated to be 360 mS/mm (extrinsic 275mS/mm) and the minimum on-resistance is R_{on}=2Ωmm. A typical DC-IV output characteristic with the drain current I_d normalized to the gate width w is shown in Figure 1.

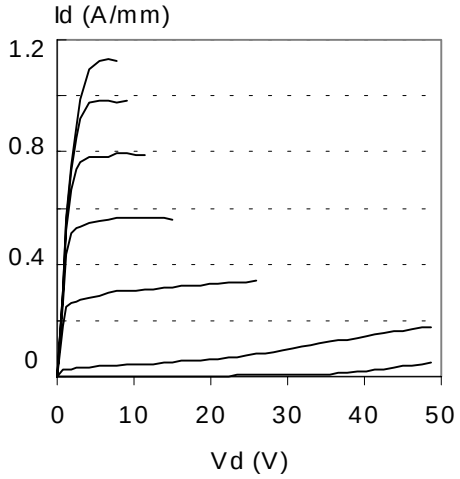

Fig.1: DC-IV output characteristic of a 2×50µm device.

SMALL SIGNAL PARAMETERS

S-parameters of the microwave power transistors were measured up to 50 GHz. For the L_G = 0.28 µm gates a typical current gain cut-off frequency f_t of 37 GHz is obtained. Therefore, the $L_G \times f_t$ product is 10 GHz×µm. This compares well with the 0.5 µm gates were we measured f_t of 21 GHz. Roll-off for the $|h_{21}|^2$-graph is around 19.5 dB/dec for all devices measured (Figure 2) and does not change with device size. Devices having 0.28 µm gate length and 100 µm gate width reveal a maximum frequency of oscillation f_{max} = 74 GHz. For larger devices (gate width w = 1 mm, L_G = 0.28 µm) f_{max} degrades to 38 GHz This indicates losses in the gate that could be reduced using T-gate technology.

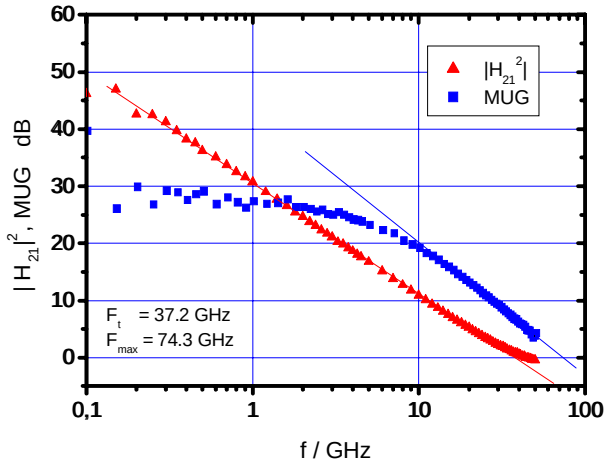

Fig.2: Current gain and maximum unilateral gain of a 2×50 µm device. (V_{GS} = -3V, V_{DS} = 20V)

LARGE SIGNAL PARAMETERS

On-wafer load-pull measurements between 2 and 10 GHz were performed using a passive system. Passive load-pull with computer controlled mechanical tuners is easy to operate but has the problem of limited access to the outer parts of the Smith-chart. The DUTs, however, are „high“ voltage transistors (V_d = 26 V) with a loadline impedance of $R_L \geq 20$ Ω. This moderate impedance is not transformed to very small values by a large parasitic output capacitance. This detrimental effect is known from LDMOS technology but the GaN HEMTs have very small output capacitances (C_{out} < 2pF @ w = 4 mm). Therefore the load matching problem is reduced and $|\Gamma_L| > 0.8$ is not required even for large gate widths. The constant value of Γ_L, given by the tuner setting, being independent of the device nonlinearity, is advantageous in particular for class B and C operation.

A typical load-pull result for the largest transistor having 0.5 µm gate length and 4 mm gate width is given in Figure 3. With operation at V_D = 26 V we reached a PAE of 53% and gain of 25dB.

For HEMTs fabricated on SiC substrates a maximum power density of 5.2 W/mm could be measured. The maximum absolute power obtained so far is 13.8 W. The simultaneously measured drain and gate currents (I_d, I_g) are shown in Figure 4. I_d increases from the quiescent value fourfold to 1 A, while the gate even at the highest input power is not driven into the forward current range.

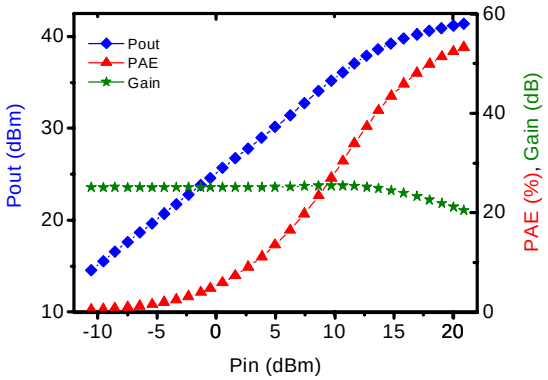

Fig.3: Power transfer characteristic of a 16×250µm device. Class A operation. f=2GHz.

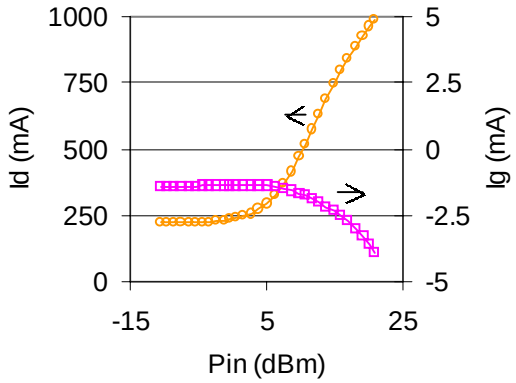

Fig.4: Bias currents I_d and I_g versus P_{in}. Same conditions as in Figure 3.

Different transistor designs with gatewidths ranging from 0.1 to 2 mm exhibit no difference in maximum power density. Only at w = 4 mm a reduction in power density was measured (Figure 5). In this case the dissipated power exceeds 10 W which probably causes overheating of the device in CW-operation. At 10 GHz the maximum power density is 4.5 W/mm but only up to w = 1mm. Obviously, the heat limit is reached earlier because PAE and Gain are much less. The PAE has decreased to 35% and the gain to 10dB.

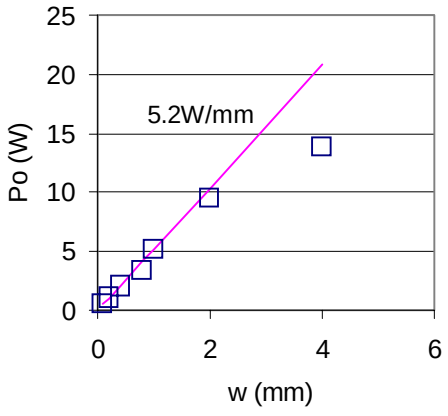

Fig.5: Constant power density up to w = 2 mm gate width. f = 2 GHz, V_d = 26 V.

PASSIVATION

It is known from AlGaN/GaN-HEMTs that max. power levels under RF-operation may differ substantially from those obtained at DC. This so-called current slump is attributed to defect states in the semiconductor at the drain side of the gate. By adding a passivation layer to the HEMT surface the rf-power may recover to a substantial degree.

An example for the power recovery from passivation is given in Figure 6 , where the increase of maximum power obtained from SiN_x-passivation is shown for a set of test devices. The HEMTs are distributed over the wafer and the average increase is 2.93 with a standard deviation of only 6.6% whereas the max. power level itself scatters by more than 12%.

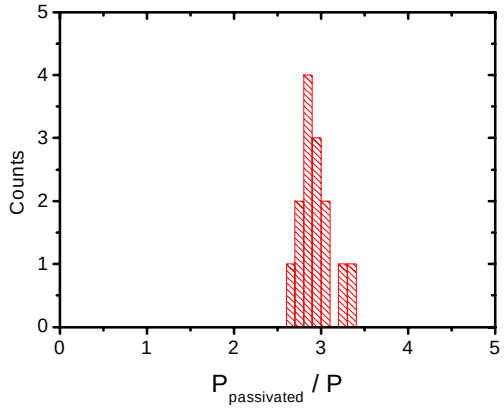

Fig.6: Statistics on the saturated power recovery ratio, given by the maximum power ratio of passivated to unpassivated devices.

In the case of AlGaN/GaN-HEMTs also polarization and piezoelectric effect play an important role and may be influenced by the passivation layer on top. We checked the influence of the piezoelectric effect by using passivation layers with different degree of mechanical stress. We used SiNx layers having a wide range of stress from compressive to tensile. Results show similar power levels for the different passivation layers, indicating that the piezoeffect does not contribute to this effect.

MAXIMUM DEVICE CURRENT

A key characteristic of the device is the peak current I_{pk} near the collector knee-voltage. Although I_{pk} seems to be accessible from DC-measurements (Figure 1), the value determined in such a way is often much higher than the maximum current under microwave excitation. In particular in GaN epi-layers various traps with low time constants cause I_{pk} to be less at RF than at DC.

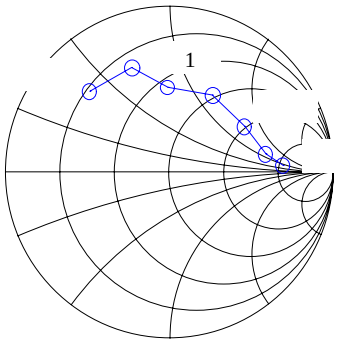

Fig.7: Γ_L for max. power. Gate width w = 0.1 – 4 mm, f = 2 GHz, V_d = 26 V.

The load resistance in a load-pull situation with maximum P_O can yield I_{pk}. Figure 7 shows the optimum load reflection coefficient Γ_L at f = 2 GHz for the investigated devices from w = 0.1 – 4 mm. From elementary loadline consideration we obtain:

$$I_{pk} = 2V_d \times \mathrm{Re}\left(\frac{1-\Gamma_L}{1+\Gamma_L}\right) \times 50 \qquad (1)$$

The result is shown in Figure 8. The peak RF-drain current of the larger devices is much less than the extrapolated DC value. Despite the proper passivation the current slump is still present. On the other hand this reduction is comparable to observations at GaAs power MESFETs, where a decline of 35% was observed. Griffin (3).

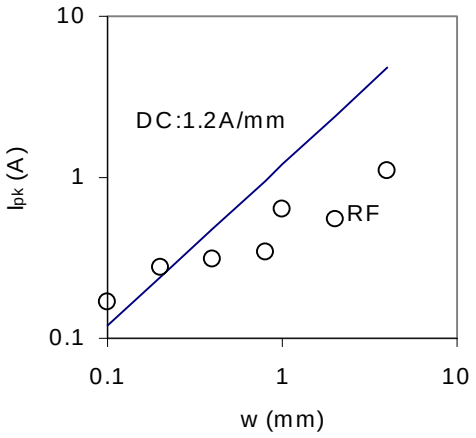

Fig.8: Device peak current I_{pk} versus gatewidth. DC measurements (solid line) and load-pull measurements (symbols).

THERMAL BUDGET ON SIC

On large periphery transistors with total gatewidth of 2 mm we investigated different thermal loading per area. For this purpose transistors of similar design except for the gate pitch, i.e. distance between gatefingers, were used. Devices under test had a gate pitch of 50 and 100 µm. They were driven into RF-saturation at 2 GHz and V_d = 26 V. In order to minimize influence of variations over the wafer always pairs from both types located in close vicinity were investigated. By testing over 20 samples we could show that the saturated power level of both transistor types is the same despite the larger area available for heat dissipation with 100 µm pitch (standard deviation 16%).
This leads to the conclusion that gate pitch may be reduced below 50 µm or the load could be increased further before a thermal limit of the device is reached.

CONCLUSION

We have developed a technology based on high throughput stepper lithography for the fabrication of large AlGaN/GaN-HEMTs on SiC substrate. A microwave power of 13.8 W @ 2GHz is achieved. Results show that the output power measured in an on-wafer load-pull setup scales linearly up to a total gatewidth of 2 mm.

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REFERENCES

(1) R. Lossy, J. Hilsenbeck, J. Würfl, H. Obloh, “Uniformity and scalability of AlGaN/GaN HEMTs using stepper lithography”, *physica status solidi (a)*, Vol. 188 (1), pp. 263–266, 2001.

(2) R. Lossy,. J. Hilsenbeck, J. Würfl, K. Köhler and H. Obloh, Proc. Int. Workshop on Nitride Semiconductors 2000, IPAP Conference Series 1, pp. 942-945, 2000.

(3) E. L. Griffin, „Application of loadline simulation to microwave high power amplifiers“, *IEEE-Microwave Magazine* Vol.1, pp.58-66, June 2000.