On the large-signal modelling of AlGaN/GaN HEMTs and SiC MESFETs

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Abstract — A general purpose LS model for GaN and SiC FET devices was developed and evaluated with DC, S, and Large Signal measurements (LS). The FET model is generalized and extended with new feature in order to improve the management of harmonics, provide a more physical treatment of the dispersion as well as delay and model other specific effects in these devices. The model was implemented in a commercial CAD tool and exhibit good overall accuracy.

I. INTRODUCTION

Wide band gap materials, such as III-nitrides or SiC, present remarkable electronic and physical properties suitable for realization of devices operating at high power-speed and high temperature. [1]-[3].

In this paper we propose a modified FET model in order to account for the specifics of AlGaN/GaN HEMTs and SiC MESFETs [1]-[4]. In specific, we introduce modifications to consider the dispersion of $g_m$ and $g_{ds}$ [5]-[8] and better description of harmonics.

The model extraction and comparison with measured data are performed on small devices ($2 \times 50 \mu m$ SiC and AlGaN/GaN) and large AlGaN/GaN devices with 1 and 2 mm total gate size.

II. DEVICE FABRICATION

All wide band gap devices used in this paper were processed in-house, process details are described in [9]-[10].

The AlGaN/GaN HEMT structure was grown by MBE on SiC by SVT Associates, Inc. The modulation doped structure consisted of a 300 Å undoped Al$_{0.2}$Ga$_{0.8}$N layer grown a 1 $\mu m$ GaN undoped GaN layer resting on a 0.3 $\mu m$ AlGaN buffer. Hall measurements showed a low field mobility of 1035 cm$^2$/Vs and 2DEG sheet carrier density of $1.38 \times 10^{13}$ cm$^{-2}$. The gate length is 0.15 $\mu m$. The saturation drain current, $I_{dss}$, was 1250 mA/mm and $g_m$ was 240 mS/mm. The extrinsic transit frequency, $f_{T,ext}$, and the maximum frequency of oscillation, $f_{max}$, are 51 GHz and 93 GHz, respectively. Small devices demonstrated a CW output power density above 3 W/mm under at 3 GHz under Class A operation for $V_{ds}=40$ V.

The SiC MESFET epi-structure was grown on a semi-insulating 4H-SiC substrate by Cree Inc. The MESFET structure consists of a 0.30 $\mu m$ p-buffer with $N_A=5 \times 10^{15}$ cm$^{-3}$, a 0.35 $\mu m$ channel with $N_D=2.8 \times 10^{17}$ cm$^{-3}$, a 0.28 $\mu m$ cap $N_D=1.6 \times 10^{18}$ cm$^{-3}$. The gate length is 0.5 $\mu m$. $I_{dss}$ is >500 mA/mm and $g_m$ is 25 mS/mm. From S-parameter measurements a $f_{T,ext}$ of 8.5 GHz and an $f_{max}$ of 32 GHz at a $V_{ds}$ of 40 V were calculated. Class A output power of more than 2 W/mm were measured at 3 GHz and $V_{ds}=50$ V.

III. TRANSISTOR MODEL

An existing current model [11] was initially used. However, better accuracy was obtained by adding three new terms, which give additional degrees of freedom to model bias dependencies of harmonics and model the dispersion in more physical way.

![Fig. 1. Measured and modelled $I_{ds}$-$V_{ds}$ of the AlGaN/GaN HEMT.](image1)

![Fig. 2. Measured and modelled $I_{ds}$-$V_{ds}$ of the SiC MESFET.](image2)
produce a model accuracy of 2-5%.

V. CAPACITANCE MODELS

In the implementation in ADS, a capacitance formulation was used directly. The small- and large-signal models are consistent and no transcapacitances are required, since the time derivatives of the charge depend only on their own terminal voltage. The resulting small-signal equivalent circuit consists of these capacitances evaluated at the corresponding DC voltage. It is important that $C_{gs}$, $C_{gd}$ are continuous functions of voltages with well defined derivatives in order to converge well in harmonic balance simulations (HB). In order to account for the specifics of the large device, the capacitance equations from [11] are appropriately modified [12] keeping the number of parameters as small as possible (15 in total).

VI. DISPERSION AND DELAY MODELLING

Conventional modelling of the frequency dispersion of $g_{ds}$ and $g_m$ is not appropriate for these types of devices, since the frequency dependence of $S_{21}$ and the maximum output power for these transistors are rather complicated. We model the dispersion in a more physical way using a back-gate approach [5]-[8]. In this case the RF feedback voltage, $V_{bg}$, is directly controlling the RF voltage at the gate and provides an adequate small-signal and large-signal description.

The delay network ($C_{del1}$, $C_{del2}$, $R_{del}$), connected at the input (Fig. 3) provides a good description of high frequency delay effects. At high frequency, the capacitance $C_{del1}$ shunts the input and directly decreases the magnitude of the control voltage $V_{gsc}$ and introduces the observed delay. The value of the delay capacitance was found by fitting the S-parameters and is very low (2-3 fF), it could thus be the capacitance of the gate footprint. The time constant $C_{del}R_{del}$ will determine the frequency at which the high frequency and high power limitations occurs. The frequency dependence of the output power can be tuned using the capacitance $C_{del2}$. Both delay capacitors $C_{del1}$ and $C_{del2}$ are quite similar, which is why, for simplicity, they were considered equal.

The SiC devices exhibit effects which can be found in some GaAs FET, like an increase of magnitude of $S_{21}$ vs. frequency. These effects are due to the influence of the channel on the spreading resistance $R_s$ which partly shunts $R_s$ (Fig. 2). I.e. $R_s$ is defined as:

$$R_s = R_{s1} + R_{s2} = A \cdot R_{s1} + (1-A)R_s$$

VII. EXPERIMENTAL EVALUATION

It is important to evaluate the device at biases along the typical load line. Multi-bias S-parameter measurements were performed splitting the measurements in two ranges

$\ldots$

where $\psi_p$ is a power series function centered at $V_{pk}$

Three new terms in comparison to [11] are introduced in this model: $K_{bg}$ which controls the dispersion via the intrinsic gate voltage at RF; $\Delta P_2$ and $\Delta P_3$, Eq. 5 which account for the $2^{nd}$ and $3^{rd}$ harmonic dependence with $V_{dr}$. The temperature dependence is modelled as a temperature dependence of $P_i(T)$, which describes the temperature dependence of the carrier velocity whereas the temperature dependence of $I_{pk}$ reflects the thermal effect on the carrier’s concentration.

This definition is more flexible than the single $P_1$ dependence as it is in [11] and allows modelling of both decrease and increase of the transconductance parameter $P_1$ with the drain voltage. Typically the three terms of the gate power series $\psi_p$ produce a model accuracy of 2-5%.

$V_{pk}$ and $I_{pk}$ are the gate voltage and the drain current at which the maximum transconductance occurs. $\alpha$, $\alpha_1$ are the saturation parameters, and the $\lambda$-parameter accounts for channel length modulation. The bias dependence of some parameters, like $V_{pk}$ and $P_1$, $P_2$, and $P_3$ is accounted for in Eq. 4 and 5. The number of parameters for $I_{pk}$ is low (11 in total) and most of them can be determined directly from measurements and used as good starting values for optimizations. Our modelling approach thus allows us to use a simple extraction procedure and extracted parameters are trimmed directly using the CAD tool optimizers.

IV. IDS MODEL

The modified current equations are:

$$I_{ds} = 0.5 \cdot (I_{dnp} - I_{dno})(1); P_1 = g_m \cdot \frac{I_{pk}}{I_{ds}};$$

$$I_{dnp} = I_{ps0} \cdot (1 + tanh(\psi_p) \cdot (1 + tanh(\alpha_s \cdot V_{ds}) \cdot (1 + \lambda_s \cdot V_{ds}) \cdot \exp(V_{ds} - V_{Tr})))(2);$$

$$I_{dno} = I_{ps0} \cdot (1 + tanh(\psi_p) \cdot (1 + tanh(\alpha_s \cdot V_{ds}) \cdot (1 - \lambda_s \cdot V_{ds}) \cdot \exp(V_{ds} - V_{Tr})))(3);$$

$$\psi_p = P_{1m}(V_{gs} - V_{pk}) + P_{2m}(V_{gs} - V_{pk})^2 + P_{3m}(V_{gs} - V_{pk})^3; (4);$$

$$\psi_n = P_{1m}(V_{gs} - V_{pk}) + P_{2m}(V_{gs} - V_{pk})^2 + P_{3m}(V_{gs} - V_{pk})^3;$$

$$V_{pk}(V_{ds}) = V_{pk} - \Delta V_{pk} + \Delta V_{pk} \cdot tanh(\alpha_s \cdot V_{ds} + K_{bg} \cdot V_{gsc});$$

$$\Delta V_{pk} = P_{1m}(f(T))(1 + tanh(\alpha_s \cdot V_{ds})); (5a);$$

$$P_{2m} = P_{2m}(1 + tanh(\alpha_s \cdot V_{ds}));$$

$$P_{3m} = P_{3m}(1 + tanh(\alpha_s \cdot V_{ds})); (5c);$$

$$\alpha_s = \alpha_s + \alpha_s \cdot (1 + tanh(\psi_n));$$

$$\alpha_s = \alpha_s + \alpha_s \cdot (1 + tanh(\psi_n)); (6)$$
of voltages; low $V_{ds}$ with high currents and high $V_{ds}$ with small currents.

Some results for measured and modelled S-parameters for 100 μm gates GaN and SiC are shown in Fig. 4-7.

Fig. 4. Measured and modelled $S_{11}$ and $S_{21}$ of the AlGaN/GaN HEMT.

Fig. 5. Measured and modelled $S_{12}$ and $S_{22}$ of the AlGaN/GaN HEMT.

Fig. 6. Measured and modelled $S_{11}$ and $S_{21}$ of the SiC MESFET.

Fig. 7. Measured and modelled $S_{12}$ and $S_{22}$ of the SiC MESFET.

It is interesting to compare some parameters that are common for all models. The current $I_{pk0}$ at which is the peak of the transconductance depends on the saturated current respectively the device size in mm. Typically $I_{pk0}=0.3-0.6$ A·mm.

The ratio between the transconductance $g_m$ and $I_{pk0}$ $P_1=g_m/I_{pk0}$ is an invariant measure of the sensitivity of the transistor current to the gate voltage.

The capacitance gate and drain nonlinear parameters $P_{11}$, $P_{21}$ are connected with the current parameter $P_1$. I. e. in a similar way the capacitances are much more linear and the nonlinear capacitance parameters are much smaller in comparison with ordinary GaAs MESFET and HEMTs. This, together with the high breakdown voltage, allows these devices to be used in high voltage or high linearity amplifiers and mixers.

VII. CONCLUSIONS

A general purpose large-signal modelling approach for GaN and SiC was proposed, implemented in ADS and experimentally evaluated. The model exhibits good accuracy, agreement and stable behaviour in HB simulations.
REFERENCES


[12]. ADS user manual