A Microstrip X-Band AlGaN/GaN Power Amplifier MMIC on s.i. SiC Substrate

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***Abstract* — A two-stage high-power amplifier MMIC was realized with a chip size of 4.5 mm x 3 mm operating between 8 GHz and 10 GHz based on a fully integrated microstrip AlGaN/GaN HEMT technology on s.i. SiC substrate. The MMIC device delivers a maximum pulsed output power of 8.9 W (39.5 dBm) at 8.5 GHz at V_{DS} = 31 V, 10 % duty cycle, and more than 6 dB gain compression level, and features a linear gain in excess of 20 dB.**

I. Introduction

In recent years, significant progress has been made in III-N device technology [1, 2]. In the development from devices to integrated circuits for GaN HEMT technology on different substrates as SiC or silicon, passive MMIC technologies enabling the realization of e.g. MIM capacitors, resistors and inductances were adapted to these substrates [3,4]. Recently, various GaN on SiC power amplifiers (e.g. [3]) and hybrid microstrip amplifiers with GaN HEMTs (e.g. [5]) with encouraging performance were realized. For MMIC compatibility with radar modules in hybrid microstrip technology and simple RF grounding schemes in high-power amplifier MMICs, microstrip technology on thinned substrates is preferred [6]. An outstanding realization of a microstrip GaN HEMT process on s.i. SiC substrate with impressive RF power data is reported e.g. in [6]. The obvious advantages of this technology for HPAs are the superior power density of GaN HEMTs and the high thermal conductivity of the SiC substrate. This work presents a microstrip two-stage high power MMIC amplifier operating between 8 GHz and 10 GHz suitable for phased array radar applications in X-band with a chip size of 13.5 mm^2.

II. AlGaN/GaN HEMT Technology

The AlGaN/GaN HEMT technology is based on two inch semi-insulating SiC wafers and multi-wafer MOCVD III-N epitaxy for active device layer fabrication. The gates of the AlGaN/GaN single heterojunction devices are defined by electron beam lithography. For X-Band applications, we use 300 nm gatelength, which gives a typical transition frequency of more than 36 GHz for a FET cell with 1 mm total gatewidth. The HEMT structure yields a low knee voltage of 5 V and a breakdown voltage BV_{DS} of 65 V allowing for a maximum DC operating voltage of 35 V. The low-frequency dispersion effects of the active devices are minimized by careful optimization of the passivation. A two-level metallization and airbridge process completes the frontside processing. This MMIC process is fully compatible with the subsequent backside process and features metal-insulator-metal (MIM) capacitances with a breakdown voltage of 200 V, inductances, and NiCr resistors. The passive circuit elements are realized using thick galvanic gold which ensures sufficient current handling capability for a microstrip power MMIC process.

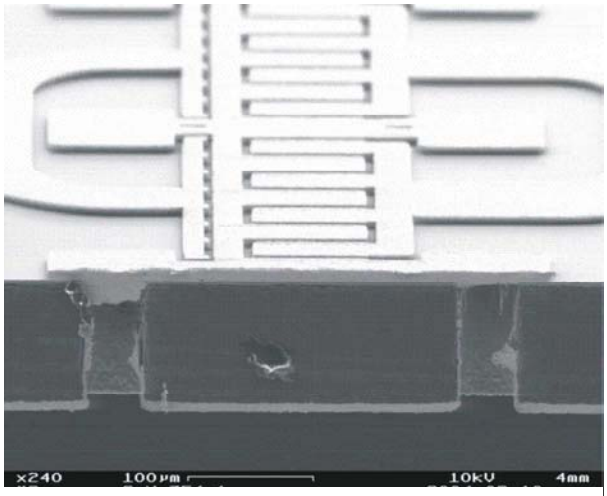

Fig. 1 Cross-section of etched via holes in 100 µm thick SiC substrate with galvanic Au backside metallization and frontside HEMT structure.

III. Microstrip Backside Process Technology

After frontside processing, the wafers are mounted on a suitable carrier. The SiC substrate is thinned to 100 µm by mechanical polishing. An etch mask is deposited on the backside surface of the wafers and is structured in an optical photolithography step. 50 µm square vias are etched through the SiC substrate using dry etch. The vertical cross-section of the vias is also rectangular. There is no significant under-etching of the mask. After the etch step, this mask is removed and a backside metallization step with thick galvanic gold is applied. Fig. 1 depicts a SEM picture of the cross-section of typical via holes in the SiC substrate which have a good

vertical shape together with a sample frontside HEMT structure. The remnants of gold metallization in the via cross section remain from the mechanical splitting of the wafer.

IV. Device Modeling and Measurements

A full microstrip passive component library has been extracted from passive test wafers featuring via test structures, transmission lines, T-junctions, MIM capacitors, and inductances in addition to the standard passive elements available within Agilent ADS. The via structure was investigated in Agilent HFSS 3D structure simulation and found to be in good agreement to the measurements and the extracted lumped-element via model within ADS. The RF behavior and the low DC resistance of the vias were found to be very reproducible with a DC resistance of less than 15 mΩ. In the via model extraction, the inductance value for a 50 µm square via through the 100 µm thick SiC substrate was found to be approx. 14 pH.

For large-signal modeling of the active devices, an in-house large-signal model including frequency dispersion and thermal effects was used [7]. This model was adapted to the microstrip environment with a revised parasitics structure including the via inductances and backside ground capacitances. As a direct model verification on device level, CW load-pull measurements have been performed for power cells with Wg= 1 mm yielding a power density of 5.2 W/mm at 10 GHz, a linear gain of 13 dB, and a power added efficiency of 33 % at V_{DS} = 35V. A typical power sweep for the W_G = 1 mm device with load reflection coefficient tuned for optimum output power is depicted in Fig. 2.

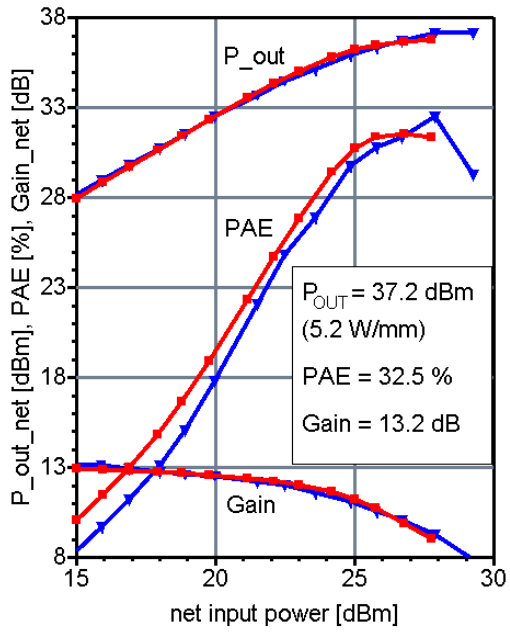

Fig. 2. Output power, PAE and gain vs. net input power for a W_G = 1 mm HEMT at 10 GHz and V_{DS} = 35 V. Measurement: Triangles (blue), Simulation: Squares (red).

Net output power, PAE and net gain are displayed vs. net input power. Measured data (blue traces, squares) and simulation with our large signal model (red traces, triangles) show very good agreement over the entire input power range.

V. Microstrip MMIC Circuit Design

A HEMT basic cell with 1 mm total gatewidth (8 x 125 µm) was chosen for the design approach. For this cell, the load-pull contours for net output power, net gain, and efficiency were obtained from an ADS simulation with our large-signal device model at 3 dB compression level for a DC drain voltage of V_{DS} = 30 V and RF input frequencies between 8 GHz and 12 GHz with 1 GHz step. The simulated net gain for maximum output power at 10 GHz is 10 dB at V_{DS} = 30 V. Therefore, an amplifier design goal of 18 dB gain and ≥10 W output power requires a two-stage design with a total gatewidth of 4 mm (four FET cells) in the final stage and 2 mm (two FET cells) in the input stage.

Instead of a parallel connection of two amplifier branches having e.g. two of four base cells in each final stage, we follow a modular concept using two separate stages comprising four-way splitters in the final stage and two-way splitters in the driver. This corresponds to three passive combiner and matching networks which are designed using mirror devices after [9] based upon the values of the optimum load and source reflection coefficients which were obtained from the above load-pull simulations at different frequencies.

The output matching network (OMN) is designed to transform the external 50 Ω load near the optimum load impedance for maximum power output at the drain reference planes of the four FET base cells of the PA stage. The input matching network (IMN) and the interstage matching network (ISMN) are designed for best matching near the upper band edge, yielding to a sufficient flat gain response. In addition, a "forced matching" using a 50 Ω parallel resistor is introduced at the RF input side of the IMN to improve the matching at the lower band edge and to ensure the "outband" stability of the entire two-stage circuit. For the upper band edge, the forced matching is made ineffective by means of a parallel resonator circuit. As an important final design step, a circuit stability check using Z parameter ports at gate and drain of each FET as described by Ohtomo [8] is performed.

The above-mentioned passive microstrip library is used especially for elements for which no model elements exist in ADS, e.g. special MIM capacitors. The coupling of adjacent microstrip structures is taken into account by performing a structure simulation as final design step (2.5D simulator for planar structures, ADS momentum) for proper description of rather compact MMIC circuits. An ADS passive microstrip element library is adapted to our technology and significantly speeds up the design and layout process using the automatic layout generation feature within ADS.

For our AlGaN/GaN HEMTs, the optimum load impedances, which were determined as first step of the

design procedure, agree very well with a parallel connection of the "Cripps" resistance and an inductive reactance. The latter is calculated from the negative small-signal output capacitance which is the sum of drain-source capacitance C_{ds} and gate-drain capacitance C_{gd} which were extracted from small-signal S-parameters up to 10 GHz. This comparison is depicted in polar representation in Fig. 3 for the frequency range from 5 GHz to 12 GHz.

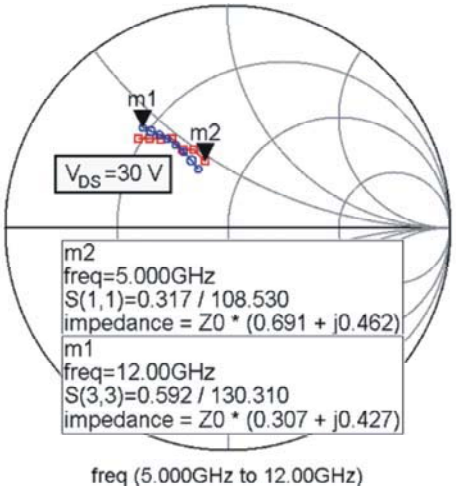

Fig. 3 Optimum load impedance vs. frequency: Large-signal simulation (squares) vs. small-signal "reactive Cripps" approach (circles) for V_{DS} = 30 V between 5 GHz and 12 GHz.

VI. MMIC Small-Signal Performance

Fig. 4 shows a chip photograph of the two-stage high-power microstrip amplifier MMIC. The chip size is 4.5 mm x 3 mm, including large-area bias decoupling capacitors and DC bias pads for direct on-wafer test. The measured CW S-parameters of the amplifier are investigated at different DC drain voltages (V_{DS} = 15, 20, and 25 V) and gate voltage adjusted for rather small drain currents below the maximum of the transconductance (V_{GS} = -5 V). As depicted in fig. 5, the output reflection coefficient is better than 8 dB from 7 GHz to 12 GHz, the input match is better than 8 dB between 9 GHz and 11 GHz. A maximum S_{21} of 18 dB is measured at 8.5 GHz in CW mode at V_{DS} = 15 V and decreases to 16.5 dB at V_{DS} = 25 V at this gate bias. The reflection parameters S_{11} and S_{22} are rather insensitive to a change of the drain voltage. From 8 GHz to 10 GHz, the gain is larger than 15 dB. The reverse isolation is better than -40 dB for all frequencies.

VII. Pulsed Large-Signal Measurements

A power sweep under RF- and DC pulsed operation of the MMIC is presented in fig. 6. These measurements were performed on different samples with a HP8510 network analyzer with "pulsed-RF" option and an Agilent 85124 pulsed bias system. The quiescent bias conditions were set to "cold pinch-off" (V_{DS0} = 0 V and V_{GS0} = -7 V), the on-state bias was near the maximum transconductance for V_{GS}, and a drain voltage of V_{DS} = 31 V. The pulse duration was 100 µs with 10 % duty cycle. With a maximum input power of 24 dBm at a frequency of 8.5 GHz, an output power of 39.5 dBm was measured with a gain compression of more than 6 dB referenced to a small-signal gain of 21 dB, i.e. the power gain is 15.5 dB. In large-signal operation, the efficiency at maximum power is more than 20 %. The noise in the power sweep curves in fig. 6 for low and medium input power levels is related to the limited dynamic range of the pulsed-RF measurement system. The maximum measured output power under pulsed-RF operation is 1 dB below the simulated value, and the measured gain compression level is 0.5 dB below the simulated value. The difference in the maximum output power is mainly due to residual losses in the passive microstrip output combiner and matching network which are not covered in the structure simulation of this circuit part.

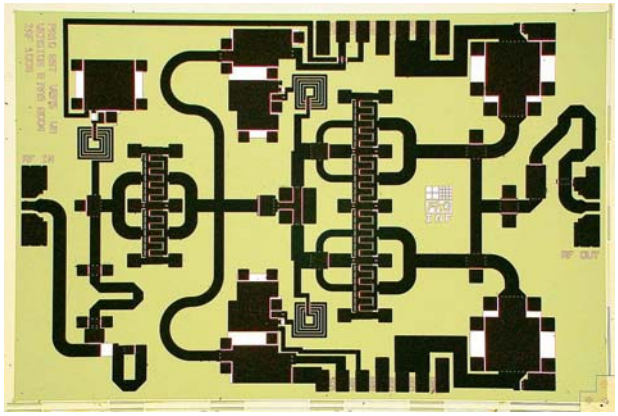

Fig. 4 Chip photograph of the two-stage microstrip X-band MMIC amplifier. Chip size is 4.5 mm x 3 mm.

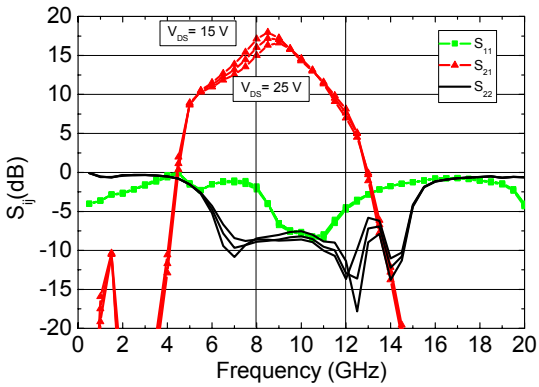

Fig. 5 Measured S-parameters vs. frequency in CW mode for the two-stage microstrip HPA at V_{DS} = 15, 20, and 25 V.

Fig. 7 displays the maximum output power and the small-signal gain vs. the DC drain pulse voltage for the above pulsed-RF power sweep measurement at 8.5 GHz. The output matching was optimized for maximum output power at a drain voltage of V_{DS} = 30 V. Output power

and linear gain were measured up to a pulsed drain bias of V_{DS} = 33 V. For a drain bias of V_{DS} = 15 V, the output power decreases to 31.5 dBm. A decrease of 6 dB in saturated output power would be expected for an ideal "Cripps" load and zero knee voltage if the drain voltage is reduced by a factor of two. The measured decrease in output power is approx. 8 dB in the range from V_{DS} = 31 V to V_{DS} = 15 V due to the non-zero knee voltage of the real device.

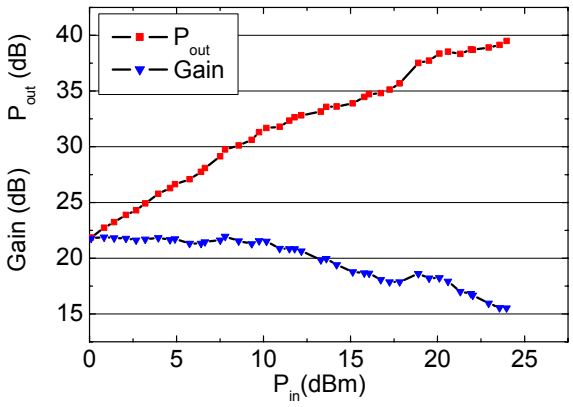

Fig. 6 Pulsed output power and gain measurement at V_{DS0} = 31 V with a pulse length of 100 µs and 10 % duty cycle at f = 8.5 GHz.

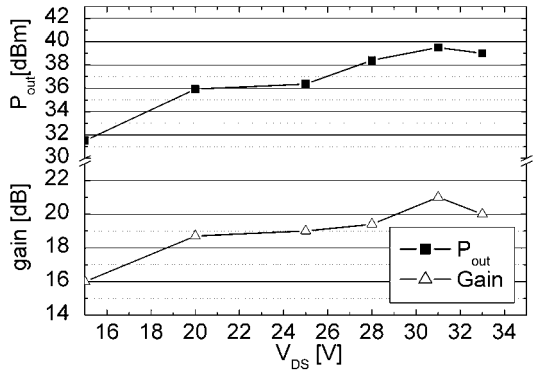

Fig. 7 Maximum pulsed-RF output power and small-signal gain vs. pulsed drain bias voltage at 8.5 GHz.

VIII. Conclusions

A microstrip AlGaN/GaN HEMT MMIC technology on semi-insulating SiC substrate including a complete backside processing, i.e. substrate thinning and via hole etching, was developed. A high-power two-stage microstrip MMIC amplifier intended for radar applications in X-band was demonstrated in this technology. Covering the frequency band from 8 GHz to 10 GHz, the maximum pulsed output power with 10 % duty cycle and a pulsed drain voltage of V_{DS0} = 31 V was 39.5 dBm (8.9 W) while the maximum linear gain was more than 20 dB. The maximum efficiency is larger than 20 %. The presented results are obtained from a first design cycle and are encouraging for future X-Band radar applications. However, future circuit design work will be directed to improved PAE and increased bandwidth, and reliability will be further investigated to enable full use of the high power density of the AlGaN/GaN HEMTs in the microstrip environment.

Acknowledgement

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References

[1] J. W. Palmour, J. W. Milligan, J. Henning, S. T. Allen, A. Ward, P. Parikh, R. P. Smith, A. Saxler, M. Moore and Y. Wu, "SiC and GaN Based Transistor and Circuit Advances", Proc. GAAS 2004, Amsterdam, NL, pp. 555–558.

[2] Triquint Semiconductors, press release, Dec. 1, 2003, http://www.triquint.com/investors/press/dspPressRelease.cfm?pressid=174.

[3] "Malibu Lab Eyes X-band with GaN-Based MMIC", Comp. Semi., p. 19, Oct. 2004.

[4] D. M. Fanning, L. C. Witkowki, C. Lee, D. C. Dumka, H. Q. Tserng, P. Saunier, W. Gaiewski, E. L. Piner, K. J. Linthicum, W. Johnson, "25 W X-band GaN on Si MMIC", GaAs MANTECH 2005 Conf. Proc., New Orleans, USA, April 11th-14th, 2005.

[5] J. W. Lee, L. F. Eastman, and K. J. Webb, "A Gallium Nitride Push-Pull Microwave Power Amplifier", IEEE Trans. on Microw. Theory Tech., vol. 51, no. 11, Nov. 2003, pp. 2243-2249.

[6] J. W. Palmour, S. T. Sheppard, R. P. Smith, S. T. Allen, W. L. Pribble, T. J. Smith, Z. Ring, J. J. Sumakaris, A. W. Saxler, and J. W. Milligan, "Wide Bandgap Semiconductor Devices and MMICs for RF Power Applications", IEDM 2001, Washington DC, USA, Dec. 2-5, 2001, pp. 385-388.

[7] F. van Raay, R. Quay, R. Kiefer, M. Schlechtweg, and G. Weimann, "Large Signal Modeling of AlGaN/GaN HEMTs with $P_{sat} \geq 4$ W/mm at 30 GHz suitable for Broadband Power Applications", IEEE MTT-S International Microwave Symposium Digest, 2003, Philadelphia, USA, pp. 451-454.

[8] M. Ohtomo, "Stability Analysis and Numerical Simulation of Multidevice Amplifiers", IEEE Trans. on Microw. Theory Tech., vol. 41, no. 6/7, June/July 1993, pp. 983-992.

[9] S. Ramberger, T. Merkle, "A Symmetry Device to Speed Up Circuit Simulation and Stability Tests", IEEE MTT-S International Microwave Symposium Digest, 2002, Seattle, USA, pp. 967-970.