

Floating-Body Effects in AlGaN/GaN Power HFETs

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AlGaN/GaN power HFETs grown on a 200nm thick AlN sub-buffer layer are investigated. The presence of a steady kink in the static and dynamic drain-to-source current characteristics is attributed to floating-body (FB) effects that result from the AlN sub-buffer layer. A method to extract the off-state body-to-source voltage (V_{BS}) is applied and the coherence of the results confirms that FB effects are present in this type of structures. To our knowledge, this is the first time that floating-body effects are reported and modeled in AlGaN/GaN HFETs.

I. INTRODUCTION

GaN-based transistors are of great interest because they offer high power handling capabilities, and high frequency operations. Power densities up to 9W/mm and cutoff frequencies (f_T) above 60GHz have been reported [1]. However, the study of issues like the reliability of GaN-based devices is still in its early stages and is crucial to provide a mature technology. In a wurtzite crystal structure, the lateral lattice constant of AlN ($a = 3.11\text{\AA}$) is an intermediate between the one of SiC ($a = 3.086\text{\AA}$) and the one of GaN ($a = 3.189\text{\AA}$). Therefore, in order to reduce the stress due to the lattice mismatch, and to improve the quality of the GaN buffer layer, an AlN sub-buffer layer is grown between the SiC substrate and the GaN buffer layer, resulting in higher device performance and reliability [2-4].

We report the study of AlGaN/GaN HFETs grown on SiC substrates with an AlN sub-buffer layer. A method to extract the off-state body-to-source voltage is applied to the device, and the coherency of the results confirms that floating-body effects are present in these structures and result from the AlN sub-buffer.

II. EVIDENCE OF FLOATING-BODY EFFECTS

At 300K, the bandgap of AlN is 6.2eV, its low frequency dielectric constant is $\epsilon^{AlN} = 8.5 \cdot \epsilon_0$, and its resistivity, ρ^{AlN} , is larger than $10^{14} \Omega \cdot \text{cm}^{-1}$. These semiconductor properties suggest that the body of the GaN-based devices is formed on an insulator. Fig.1 illustrates the structure of the considered devices. Since no contacts are fabricated between the body and the source, some properties similar to

thin-film Silicon On Insulator (SOI) ($\epsilon^{SiO_2} = 3.9 \cdot \epsilon_0$, $\rho^{SiO_2} > 10^{14} \Omega \cdot \text{cm}^{-1}$) are expected [5].

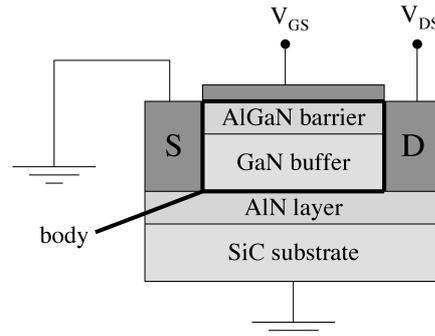


FIG. 1: Layer structure of AlGaN/GaN HFETs.

When no contacts are fabricated between the body and the source, a kink is present in the current characteristics due to the existence of a body-to-source voltage V_{BS} that affects the threshold voltage. As shown in Fig.2, a kink is observed in the current characteristics of the HFETs. This kink has already been measured in similar AlGaN/GaN devices but has not been studied [6,7].

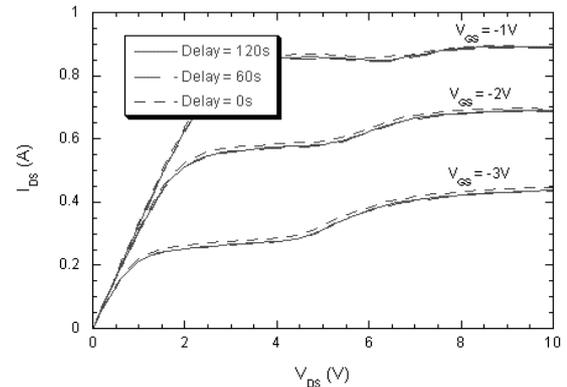


FIG. 2: DC-IV characteristics of a AlGaN/GaN HFET with AlN sub-buffer layer on SiC substrate.

When buffer-trapping effects are dominant, adding a delay between each drain-to-source voltage sweep gives time for the trapped carriers to relax, and the current characteristics become kink-free. In those devices, a delay of 2 minutes does not yield to a kink-free characteristic. In addition, pulsed-IV measurements (Fig.3) are performed and results still exhibit a current kink. Based on this measurement analysis, we attribute floating-body effects as the source of the kink.

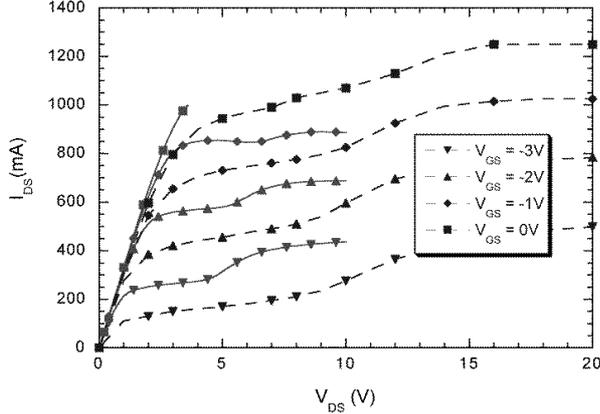


FIG.3: Pulsed-IV characteristics of a AlGaIn/GaN HFET with AlN sub-buffer layer on SiC substrate.

III. MODELING OF FLOATING-BODY EFFECTS

We propose to apply a method used in SOI technology [8] to extract the off-state FB voltage of our AlGaIn/GaN HFETs. When the gate bias (V_{GS}) is below the threshold voltage (V_{TH}) the channel resistance is large and the transistor can be represented with the T-circuit shown in Fig.4.

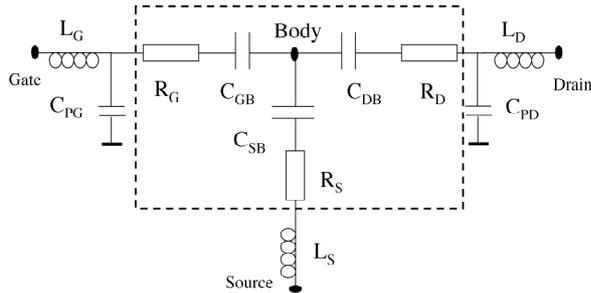


FIG.4: Equivalent circuit for large value of channel resistance.

The parasitic capacitances (C_{PG} and C_{PD}) and the parasitic inductances (L_D , L_G , L_S) result from the metal traces and the probing pads, their values are bias independent and are determined using conventional on-wafer de-embedding methods [9-10]. The parasitic capacitive and inductive elements are de-embedded from the measured S-parameters, which are then converted to the Z-parameters. The remaining resistive and capacitive

elements of the model are extracted at various V_{DS} for $V_{GS} < V_{TH}$ with the following set of equations:

$$\begin{aligned} Z_{11} &= R_G + R_S + \frac{1}{j\omega} \cdot \left[\frac{1}{C_{GB}} + \frac{1}{C_{SB}} \right] \\ Z_{12} &= Z_{21} = R_S + \frac{1}{j\omega} \cdot \left[\frac{1}{C_{SB}} \right] \\ Z_{22} &= R_D + R_S + \frac{1}{j\omega} \cdot \left[\frac{1}{C_{DB}} + \frac{1}{C_{SB}} \right] \end{aligned} \quad (1)$$

Where R_G , R_S , and R_D are the parasitic resistances and are associated with the technology and device geometry of the gate, source and drain, respectively. C_{SB} represents the source-body junction capacitance, C_{DB} the drain-body junction capacitance, and C_{GB} the gate-body capacitance. Once the source-body junction capacitance is extracted, the FB voltage is determined using the PN junction capacitance model:

$$C_{SB}(V_{SB}) = \frac{C_{J0}}{\left[1 + \frac{V_{SB}}{V_J} \right]^m} \quad (2)$$

Where C_{J0} is the zero bias junction capacitance, V_J the junction built-in potential, m the junction grading coefficient, and V_{SB} the FB voltage. This expression can be rewritten as:

$$V_{BS} = V_J \cdot \left[\frac{C_{J0}}{C_{SB}} \right]^{1/m} \quad (3)$$

Before using this relation, parameters V_J , C_{J0} , and m must be determined. As presented in [8] the capacitance C_T that results from the series connection of C_{SB} and C_{DB} can be extracted from measured Z_{22} , and can also be approximated in a first order by:

$$C_T = \frac{1}{\frac{1}{C_{SB}} + \frac{1}{C_{DB}}} \approx \frac{C_{J0}}{1 + \frac{V_{DS}}{V_J}} \quad (4)$$

This expression can be rewritten as:

$$\frac{C_T}{C_{J0}} \approx \frac{1}{1 + \frac{V_{DS}}{V_J}} \quad (5)$$

Fig.5 illustrates the extraction of C_{J0} , V_J and m . Best fit analysis gives $C_{J0} = 853\text{fF}$, $V_J = 1.75\text{V}$ and $m = 0.11$.

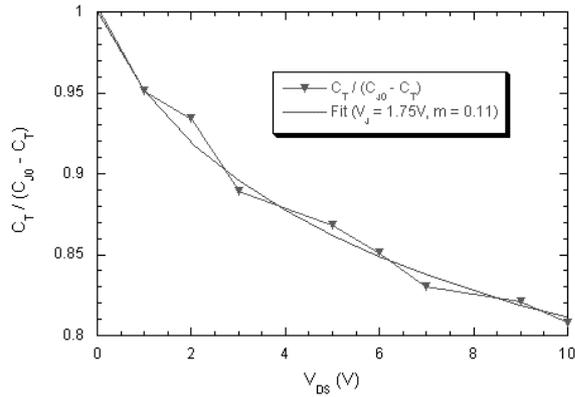


FIG.5: Plot of measured and modeled drain-source C-V data based on Eqn.5 for extraction of parameters m and V_J .

Finally, Fig.6 and Fig.7, show the extracted capacitances and the off-state FB voltage of the device, respectively.

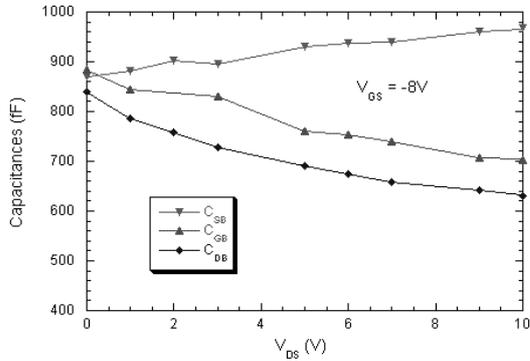


FIG.6: Extracted capacitances values versus drain voltage.

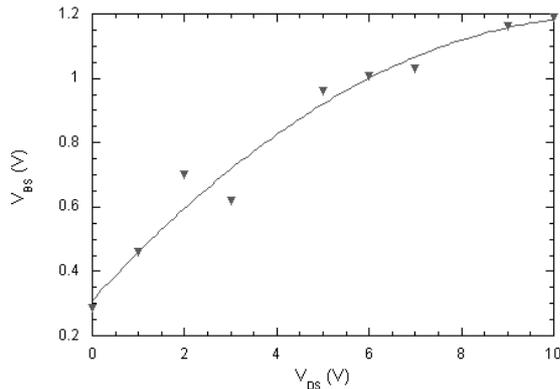


FIG.7: Extracted off-state body-to-source voltage versus drain bias.

IV. CONCLUSION

The use of an AlN sub-buffer layer in an AlGaIn/GaN structure improves the quality of the GaN buffer layer. However this added sub-buffer layer yields to effects similar to the ones observed in SOI technology. Some of these effects are undesirable and it is important to understand them

for improvement in device maturity. We reported the existence of floating-body effects in the studied AlGaIn/GaN HFETs grown on a 200nm thick insulating AlN sub-buffer layer, and we extracted the off-state body-to-source voltage. To our knowledge, this is the first time that floating-body effects are reported and modeled in GaN-based FETs.

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