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A GaAs HBT Emitter-Injected Upconverter at Ka-Band

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ABSTRACT

This work reports on the design and measured performance of a single-ended upconverter at Ka-band. The upconverter uses a 6.5x3μm^2 GaInP/GaAs HBT as the nonlinear mixing element. The LO is injected into the emitter of the HBT, the IF is applied to the base, and the RF is extracted from the collector. This topology utilizes all three ports of the transistor and avoids the need for a diplexer or other method of combining or separating the signals. The IF, LO, and RF frequencies are 3.6 GHz, 26.5 GHz, and 30.1 GHz respectively. The measured conversion loss was less than 2dB at the center of the band while the third order intercept point was -2dBm. These results were obtained with an LO power of only -2dBm. The overall chip size is 3.7x2.5mm^2.

INTRODUCTION

The GaAs HBT possesses significant advantages over the GaAs FET in power amplifier and low phase noise oscillator applications due to its high power handling capability and low 1/f noise properties, respectively [1,2]. These characteristics make the HBT well suited for use in the transmit side of microwave and millimeter-wave transceivers. Its possible use as an upconverter may allow further integration of the transmit components of Ka-band transceivers. Use of GaAs HBTs as single-balanced [3] and double-balanced upconverters [4,5] has already been reported. This work describes a simple, single-ended upconverter which can be used in microwave and millimeter-wave applications. The intended application for this upconverter is an indoor Ka-band wireless local area network (WLAN).

The design approach for the upconverter will be described including the topology, biasing, and matching networks. Simulated and measured results will then be presented.

CIRCUIT DESIGN

Nortel's (Northern Telecom's) internal GaInP/GaAs HBT foundry was used for the development of the upconverter. The HBTs had an f_t and f_{max} of 60 and 75 GHz respectively. The emitter area of the HBT used in this circuit was 6.5x3μm^2. The circuit was simulated with HP-EEsof's harmonic balance program Libra™ and electromagnetic simulator Momentum™. The nonlinear model used to describe the device behaviour was that developed by Zhang et al. [6] and has been implemented in Libra™ [7]. This model includes self-heating, transit-time, and emitter barrier effects.

I Topology

In designing the upconverter, a topology was required which allowed for the injection of both the LO and IF signals as well as the extraction of the RF signal. This is often accomplished with single-ended FET mixers by using a diplexer or coupler to combine the IF and LO signals at the gate of the FET. With a drain FET mixer topology the IF is applied to the gate, the LO to the drain, and the RF extracted from the drain. This topology also would require a diplexer. In single-ended upconverters where the LO and IF frequencies are far apart it can be difficult to match both frequencies simultaneously and the combining/matching circuits can become the most challenging part of the design. Diplexers or other combining circuits can also become large and are often provided off-chip. To avoid these difficulties, all three ports of the transistor are used in this design. A block diagram of the circuit is shown in Figure 1. With this topology, the emitter, which is usually RF grounded is now utilized to inject the LO signal [8]. The transistor is in common emitter configuration.

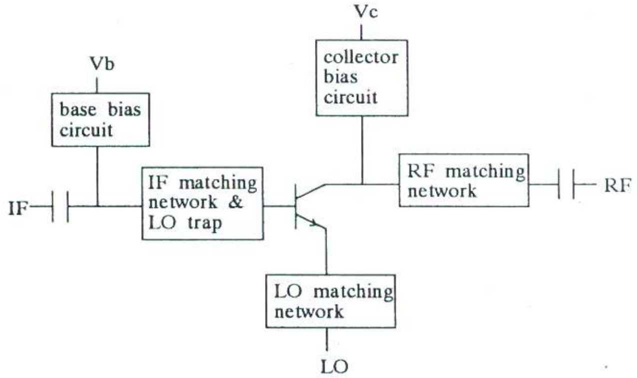

Figure 1 Block diagram of upconverter.

II Bias Point

After choosing the topology, the bias point and LO power were investigated. A number of factors were considered when choosing this point. Several simulations were performed varying the LO power and base-emitter voltage, V_{BE}, in order to find a combination which gave the best conversion gain performance while keeping the collector current, I_C, below the maximum rated value of 10.5mA. The value of V_{BE} which achieved this situation biased the transistor in cutoff where it behaves in a strongly nonlinear fashion. Simulations showed that increasing the value of V_{BE} compromised the stability of the circuit. A collector-emitter voltage, V_{CE}, value was chosen which kept the transistor's instantaneous voltage from entering the saturation region and also prevented the device from entering a thermally unstable region of operation. The circuit was measured at a bias point of V_{BE} = 1.0V and V_{CE} = 1.25V.

III Bias Circuits

The complete schematic of the upconverter showing the details of the bias and matching circuits is shown in Figure 2.

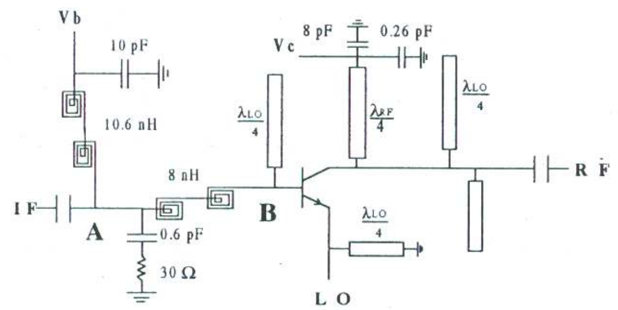

Figure 2 Schematic of upconverter showing bias and matching networks.

The base bias circuit consisted of two 5.3nH inductors connected in series to provide an IF choke. A 10pF capacitor to ground was included for bias decoupling. This bias circuit was connected in shunt in front of the matching network at point A in Figure 2 as opposed to it being connected as close as possible to the base of the HBT at point B. This was done because at point A, the impedance looking toward the base would be approximately 50Ω. The bias circuit impedance can be made much higher than 50 Ω so that it does not perturb the circuit. At point B, however, the impedance looking into the base of the HBT was very high and the bias circuit impedance would load the circuit.

In the collector bias circuit a 0.26pF capacitor resonates with the via inductance at 30.1GHz in order to provide a short circuit at the RF frequency. The $\lambda_{RF}/4$ stub transforms the short circuit to an open circuit at the point where it connects to the collector side of the HBT. An 8pF capacitor was also connected in shunt to provide bias decoupling and provide a short circuit at the IF frequency to reduce IF leakage into the RF port.

IV Matching Networks

The LO matching network was designed first. A $\lambda_{LO}/4$ open circuit stub at the LO frequency was connected in shunt to the base of the transistor in order to prevent any LO signals from entering the IF port. It also eases the matching at the LO port because it reduces the sensitivity of the LO impedance at the emitter port to any IF matching circuitry connected to the base. It was found that the return loss (RL) at the LO frequency looking into the emitter was better than 11 dB which was deemed acceptable and thus no further matching was added. Only a short-circuit shunt stub, $\lambda_{LO}/4$ long, was needed in order to provide a DC ground to the transistor and not perturb the LO match. This does, however, reduce the conversion gain of the mixer due to the fact that the $\lambda_{LO}/4$ causes series inductive feedback at the IF frequency.

The IF impedance looking into the base of the HBT was very high due to the cutoff bias situation. It was determined that simple reactive matching would result in an extremely narrow bandwidth. To overcome this, a lossy matching network (see Figure 2) was used in order to increase the bandwidth. The matching network consisted of lumped elements in order to conserve space. The spiral inductors were represented in the simulator with measured S-parameter blocks taken from previous foundry runs.

The RF matching network was designed to attenuate the LO signal at the RF port as much as possible while still providing a good match at the RF frequency. This was achieved simply by using two stubs, one to provide the LO short ($\lambda_{LO}/4$ long) and the other to match the RF signal.

An electromagnetic simulation using Momentum™ was performed on parts of the matching networks before the chip was sent for fabrication. The overall size of the chip was 3.7x2.5mm^2. A photograph of the MMIC upconverter is shown in Figure 3.

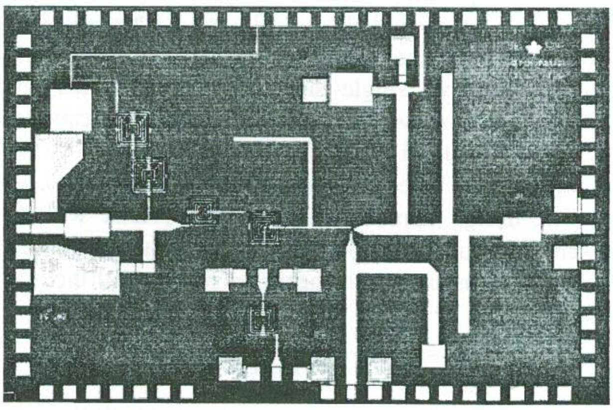

Figure 3 MMIC HBT upconverter chip.

MEASURED PERFORMANCE

The circuit was measured on-wafer using a microwave probing station. The collector-emitter voltage, V_{CE}, was set to 1.25 V and the base emitter voltage, V_{BE}, was set to 1.0 V. The IF, LO, and RF signals were 3.6 GHz, 26.5 GHz, and 30.1 GHz, respectively. The LO power was -2 dBm.

The simulated and measured IF RL is shown in Figure 4. Good agreement was obtained as the measured IF RL was shifted up in frequency by less than 5% compared with simulation. The measured and simulated RF return loss are illustrated in Figure 5. The minimum RF RL was shifted upwards in frequency by approximately 3%. This shift, however, was enough to degrade the match in the specified band of 29.85 GHz to 30.35 GHz.

The LO return loss agreed well with simulation. The measured and simulated LO return losses were 11.8dB and 10.5dB respectively.

The conversion gain across the RF frequency band is shown in Figure 6. The simulated results shows a slight gain over the band. The measured conversion gain had a peak value of -2dB and an average value of -3.5dB. One reason for the difference is the fact that the RF match was shifted up in frequency as indicated in Figure 5. As a result, the in-band RF RL was poor and thus degraded the conversion gain.

For third order intermodulation characterization, two signals were injected at 3.55GHz and 3.65GHz. The measured performance is shown in Figure 7. From extrapolation in the linear portion of the curves it was found that the third order intercept point (IP3) was -2dBm.

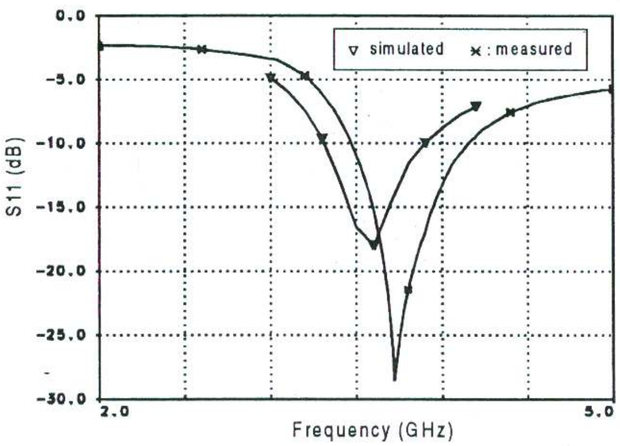

Figure 4 Simulated versus measured IF return loss.

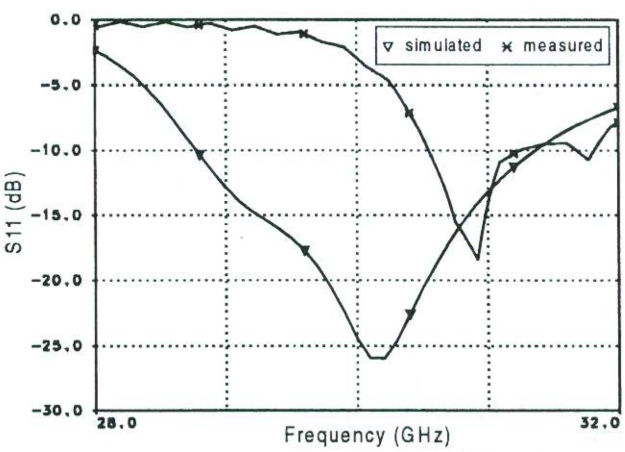

Figure 5 Simulated versus measured RF return loss.

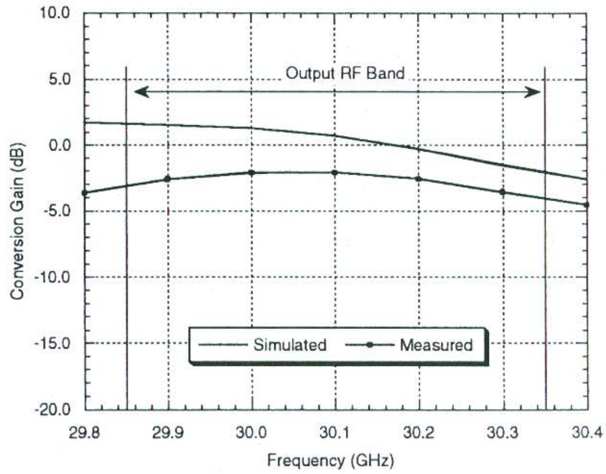

Figure 6 Simulated versus measured conversion gain.

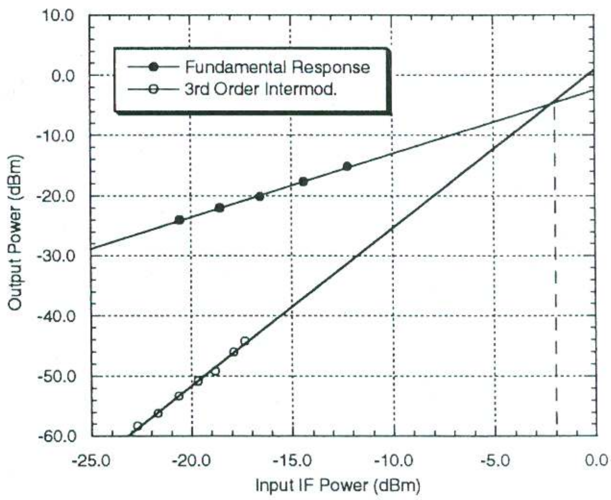

Figure 7 Measured third order intermodulation characteristic.

CONCLUSION

A GaAs HBT, single-ended upconverter MMIC with an average conversion loss of 3.5dB over the RF band of 29.85GHz to 30.35GHz and requiring only -2dBm of LO power has been presented. Injection of the LO at the emitter avoids the need for a diplexer or coupler which permits a compact and simple microwave and millimeter-wave upconverter design.

ACKNOWLDGEMENTS

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