Gallium Nitride on Silicon HEMTs for Wireless Infrastructure Applications, Thermal Design and Performance

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GaN HEMTs are being touted as the next generation microwave power transistor. Many research groups have reported outstanding DC and RF results on small periphery devices. However, the data on larger devices is somewhat limited. This paper will present results on large periphery devices (18 mm total gate width). Results from DC, RF and Linearity measurements will be presented. In addition a detailed thermal analysis based on simulation and measurement will be discussed. To our knowledge this is the first time the thermal characteristics of large periphery GaN-on-Si devices has been presented. Finally, the thermal model is used to study the thermal performance of these devices on different substrates. The results illustrate that GaN-on-Si is a viable approach for handling the large thermal dissipation requirements of microwave power transistors.

INTRODUCTION

Rapid growth in the wireless market has fueled the need for improved wireless infrastructure that can handle new bandwidth intensive applications. One crucial component of wireless infrastructure is the power amplifier, which is required to transmit signals from the cellular base station. This next generation of base stations will require power transistors with higher power, improved linearity, higher efficiency, and improved thermal management.

Gallium Nitride is an ideal fit for these applications due to its high breakdown field and high saturated electron velocity. The AlGaN/GaN heterostructure has shown sheet charge concentration greater than $1x10^{13}$ cm^{-2} and electron mobility approaching 2,000 cm^2/V-s. The combination of these properties has allowed many research groups to report record output power densities [1,2].

However, most of these results are on small periphery devices, where thermal effects are minimal. In order to commercialize this technology the devices must be scaled to large peripheries where self-heating will become an issue. The excess heat generated can cause a reduction in the power density and also impact reliability. In order to counteract thermal issues it is crucial to have the correct device layout, substrate, and backend processing.

In this paper we will discuss GaN on Si as a potential solution and show thermal imaging and simulations that validate its use at high power levels. GaN is grown directly on 100 mm Si substrates using a transition layer scheme and our proprietary MOCVD reactor design. Using this novel GaN epitaxial technology as a baseline, an AlGaN/GaN HEMT process has been developed and the resulting devices characterized for microwave and thermal performance. Results will be presented for DC, load pull, and linearity on multi-finger devices with 18 mm in total device periphery.

We will also show a thermal model developed using a commercially available finite-element software. This model has been validated with an infrared thermal imaging tool. Infrared images will be presented for multi-finger large periphery devices. To our knowledge this is the first time thermal results for large periphery GaN devices on Si have be shown.

HEMT STRUCTURE

The devices studied in this paper are based on a conservative AlGaN/GaN HEMT structure. The structure consists of a proprietary transition layer followed by an i-GaN buffer, an AlGaN region consisting of $2x10^{18}$ Si doping, and a GaN cap. The Al percentage is approximately 23%. For more details of the device structure the reader is referred to the previous publication Brown(3).

The device layout investigated consists of 90 gate fingers each with a gate length of 1.0 µm and a gate width of 200 µm, which yields a total gate periphery of 18 mm. A 30 µm pitch separates the gate fingers. The source fingers are connected with plated gold air bridges. Drain fingers and pads are also plated.

ELECTRICAL RESULTS

Figures 1, 2, and 3 show typical DC, RF, and Linearity results for these devices. The DC characteristics show approximately 10 A of drain current and a pinch-off

voltage of –4.0 V. The RF results exhibit 20 W of power with 13 dB of gain and 45% power added efficiency at 2.0 GHz. Linearity testing reveals IMD3 levels of –45 dBc at 7 dB backoff. A more detailed discussion of device linearity can be found in Nagy (4).

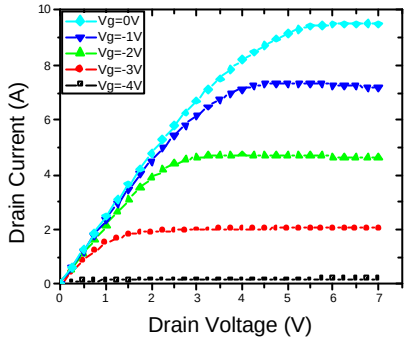

Figure 1: Output Characteristics of 18 mm Device

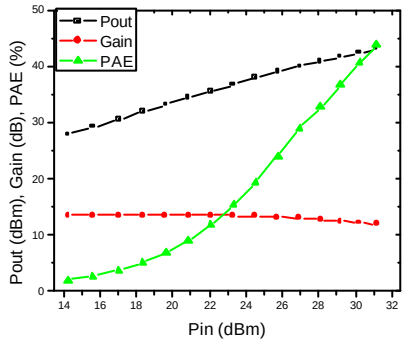

Figure 2: Power Sweep showing 20 W Power with 13 dB Gain and 45% Efficiency at 2.0 GHz

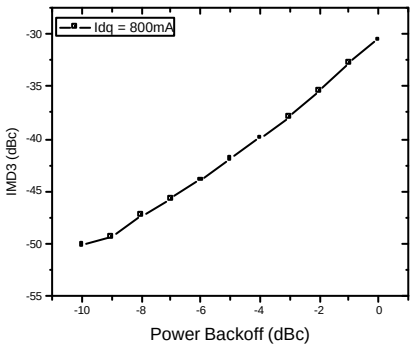

Figure 3: Linearity of 18 mm device showing –45 dBc at 7 dB backoff

SIMULATION RESULTS

Thermal simulations were performed using a three-dimensional finite-volume model. The software used was the commercially available multi-physics software, CFD-ACE+. A solution is obtained by numerically solving the conservation of energy equation in the total enthalpy form. The problem setup involves dividing the solution domain into a number of cells (or control volumes). The enthalpy equation is then numerically integrated over each of these control volumes. The solver iterates the equation until a converged solution is obtained [5].

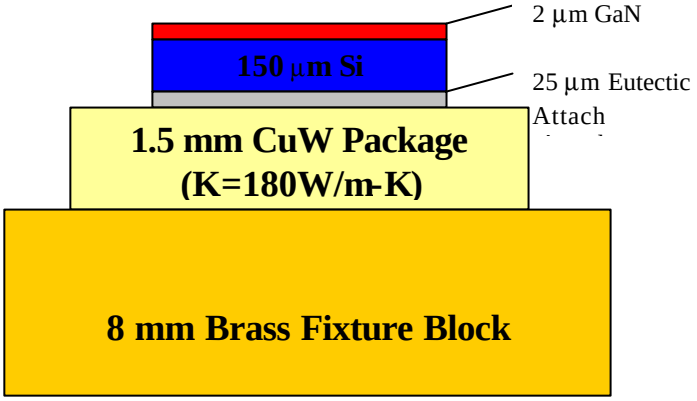

Figure 4: Block diagram showing configuration used in simulations. The base plate temperature is set at the bottom of the brass block and the junction temperature for each finger is measured in the GaN layer.

A cross-section of the simulated geometry is shown in Fig. 4.

The GaN chip measures 1 mm x 3 mm with the gate layout as described earlier. The heat dissipation is represented by a 2-D planar heat source at each of the gate fingers. Polynomial equations for the thermal conductivity of both GaN and Si are used. The package is a standard CuW RF power transistor package with a thermal conductivity of 180 W/m-K. The die attach is a Au/Si eutectic. The geometry shown above includes an 8 mm brass fixture. The fixture is included to more accurately simulate the conditions used in the IR thermal imaging measurements where the temperature is held constant at the bottom of the fixture. Alternately, the isothermal condition can be applied at the base of the package and a true θ_{JC} (junction-to-case thermal resistance) can be simulated.

Figure 5 shows the results for a power dissipation of 1.5 W/mm (or 27 W). The results show a 200^{o} C temperature at the junction. In this simulation the temperature at the base of the fixture was held constant at 80 ^{o} C (again to emulate IR imaging conditions).

Therefore, the temperature rise from fixture to junction is 120° C.

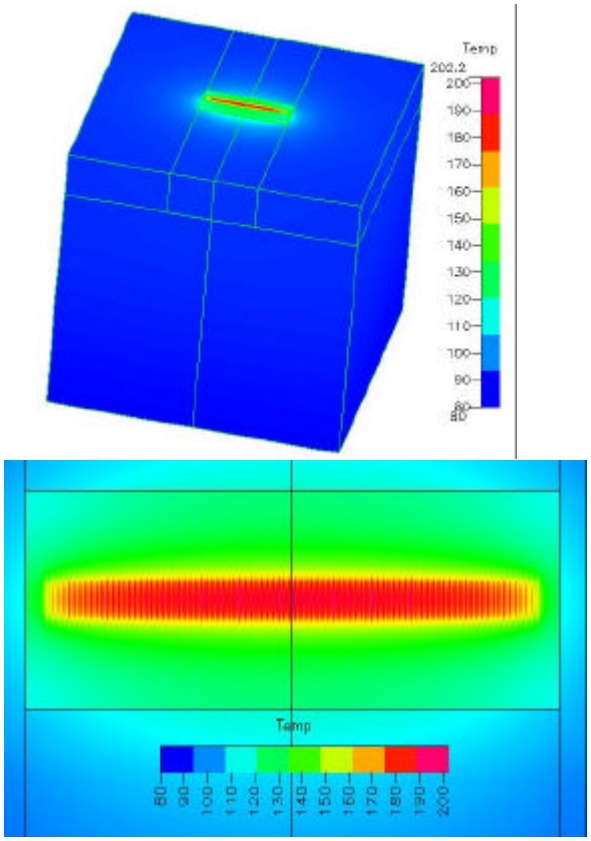

Figure 5: CFD-ACE+ Simulation showing an overview of the 18 mm geometry with package and brass fixturing block (top) and a top view (bottom) showing indivdual fingers and coupling between them

The results show coupling between adjacent gate fingers with the highest temperature rise in the middle of the chip. This finger coupling leads to a non-linear scaling of the thermal resistance with total device periphery.

THERMAL IMAGING VALIDATION

Infrared thermal imaging was chosen as an experimental technique for validating the simulation methodology. IR imaging is a widely accepted method for determining junction temperatures of high power semiconductors. All the measurements mentioned in this paper were performed at Quantum Focus Instruments using their InfrascopeII thermal microscope. The InfrascopeII can obtain spatial resolution as low as 3 µm and 0.1 milliKelvin temperature accuracy.

IR imaging is performed by measuring the radiant energy of the chip and then using a stored emissivity map to calculate the temperature. The InfrascopeII is a powerful tool that employs emissivity correction at every pixel. This is important for semiconductor materials where the large emissivity differences of the metal and semiconductor can lead to large measurement errors. Accurate measurement of the radiant energy is also required, and this dictates that the base plate temperature be elevated to 80° C [6].

The IR imaging results show a maximum junction temperature of 193 ° C (or 113 ° C temperature rise) which is very close to the 200° C predicted by the simulation. The results, as seen in figure 6, show the same finger coupling signature with the highest temperature being in the center. Experimental results from 2 different 18 mm devices are compared with simulation results at 3 different levels of power dissipation as shown in Figure 7.

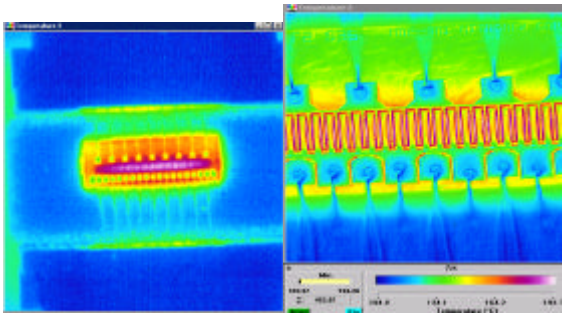

Figure 6: Thermal Imaging results of 18 mm chip with a 1X (top) and 5X (bottom) magnification

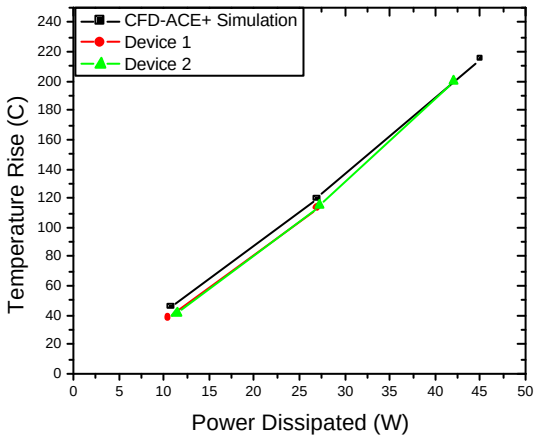

Figure 7: Comparison of Simulated results on 18 mm device with IR imaging results on 2 devices. Devices are simulated and measured at 3 different levels of power dissipation.

It can be seen that the temperature versus power curve is not linear, and thus the thermal resistance will not be constant for all power levels. In our simulations the

thermal resistance increased from 4.25 °C/W at 11W dissipated power to 4.75 °C/W at 45 W dissipated power. This non-linear behaviour is a result of the temperature dependent thermal conductivity**.**

ALTERNATE SUBSTRATES

After developing confidence in the thermal model, studies were carried out on different substrates. The purpose of these simulations was to understand how Si compares to other competing substrates from a thermal management perspective. The simulations were performed with a smaller 2 mm periphery device. The layout of this device consisted of 10 gate fingers with gate length of 1.0µm and gate width of 200µm. The gate pitch used was 25 µm. The substrate modelled was always 100µm thick and had a constant thermal conductivity. These substrate simplifications were made to speed up simulation setup and due to the lack of information available on some of the substrates.

All the simulations were carried out with a power density of 3 W/mm and the results are shown in Figure 8.

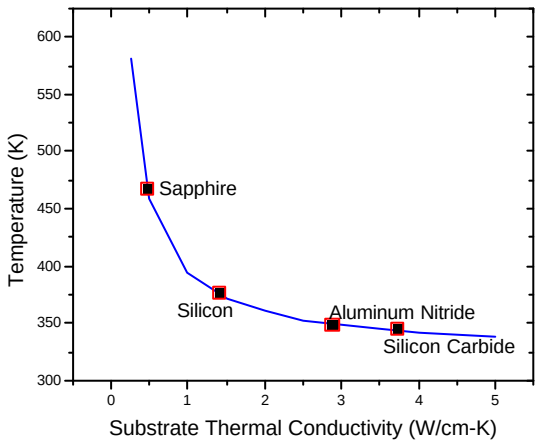

Figure 8: Comparison of junction temperature for different 100 mm thick substrates. All simulations use 10x200 mm gate finger layout with 25 mm pitch and a power dissipation of 3 W/mm.

The graph shows a 1/K dependence between junction temperature and thermal conductivity. Therefore, the benefit of high thermal conductivity substrates is limited. The finger coupling in the device and the discrete heat sources (whole die area is not powered) lead to this non-intuitive behaviour.

CONCLUSIONS

Nitronex has demonstrated the ability to grow GaN on 100 mm Si substrates. Large periphery AlGa N/GaN HEMTs processed on this material have demonstrated good DC, RF, and Linearity characteristics. A thermal model has been developed for these transistors and externally validated with IR thermal imaging. The results show that Si is a very competitive substrate in terms of thermal management. Furthermore, the low cost of Si substrates and ease of backend processing make it a very attractive choice for use in commercial GaN microwave power transistors.

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