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A monolithic GaAs clock and data recovery circuit for 2.5 Gb/s NRZ data stream

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Abstract - A GaAs monolithic clock and data recovery circuit for 2.5 Gb/s NRZ data stream has been designed and fabricated by using 0.3 μm HEMT technology from IAF FhG foundry. The main functions carried out by the IC are: signal amplification (25 dB), clock recovery and decision. The design is intended to achieve a complete 2.5 Gb/s receiver by using the IC and a LN preamplifier (transimpedance stage and limiting amplifier stage) placed in a DIL package. The overall scheme comprises about 200 active devices, used both for analog and digital blocks, uses a single rail bias (-4.5 V) and standard ECL output levels. The fabricated chip has been tested and measured by using a ceramic package and a small PCB, showing an input sensitivity of 30 mVpp and rms output jitter below 10 psec under 2^{15}-1 PRBS.

1. Introduction - The block scheme of an optical receiver comprises a transimpedance amplifier, a limiting gain stage, the clock recovery circuit and the decision circuit. A general interest is the reduction of the number of IC's required to achieve this function, in order to reduce power consumption, size and weight of the receiver board. GaAs technology is a good candidate to achieve this goal in the Gb/s data rate range, provided these problems have been managed:

1) Process parametric dispersion has not been carefully characterised in the currently available devices model libraries;
2) Cross-talk between lines is not modelled within the CAD tools;
3) Power consumption has to be reduced in order to simplify the package and the use of the chip;
4) Extremely wide fractional bandwidths of the optical systems require a very careful design of bias networks, blocking capacitors and package;
5) High gain stages and digital circuitry operate very close to each other;
6) Moreover the reduction of the number of supply voltages and external trimming pads is needed.

In this paper we present the design and the result of measurements of a 2.5 Gb/s monolithic GaAs Clock and Data Recovery circuit (CDR) which performs the following functions: voltage amplification with limiting capability, clock recovery and decision. The clock recovery is based on PLL filtering and spectral line recovery obtained by a non-linear pulse generator. This choice allows a very stable reference signal, with a low level of output jitter, but requires a frequency acquisition circuit to increase the capture range of the PLL. The design has been carried out by using IAF FhG HEMT technology with 0.3 μm enhancement/depletion devices, the overall chip size is 2 x 2 mm and the total power consumption is 1.3 W. By using this IC and a LN gain stage the integration of all the functions of the optical receiver in a DIL package becomes possible.

2. System architecture - Figure 1 shows the block scheme of the CDR. The data decision function is performed by a D-type flip-flop, driven by a limiting amplifier with the function of line receiver. The clock recovery function is based on a F/PLL loop driven by a delay line/EX-OR pulse generator. The NRZ data stream shows a null at the bit-rate frequency, so the pulse generator is used to generate a spectral line at this frequency forming a pulse at each positive or negative transition of the input signal. The PLL is used as a high Q tunable filter to select the spectral line at the bit-rate frequency. The high Q requirement gives a limited lock-in range for the PLL, so a frequency acquisition aid is necessary to ensure the clock recovery function without a VCXO; the frequency acquisition loop has been designed as a Richman's quadricorrelator [3] [4], which includes the PLL blocks (phase detector, low pass filter and VCO). Once frequency lock has been established, and the frequency difference detector output goes to zero, the quadrature phase detector (PDQ) drives the loop filter, ensuring phase acquisition. VCO reactive elements, PLL loop filters and the frequency difference detector have been placed outside the chip in order to allow fine trimming of the CDR parameters.

Limiting amplifier - The limiting amplifier is the front-end of the CDR and its function is to yield a data stream of constant amplitude to the following blocks, notwithstanding the input optical power dynamic range is close to 25 dB. The output dynamic range is close to the logic levels used by the digital circuits and the eye-diagram at the output of the limiting amplifier is widened to minimise the dependency from the clock signal phase alignment. The amplifier consists of a double stage differential voltage gain block, with a DC feedback loop with external blocking capacitors for biasing and offset compensation [2]; the input port is decoupled by off chip capacitors and the 50 Ω input matching has been obtained using the DC feedback loop.

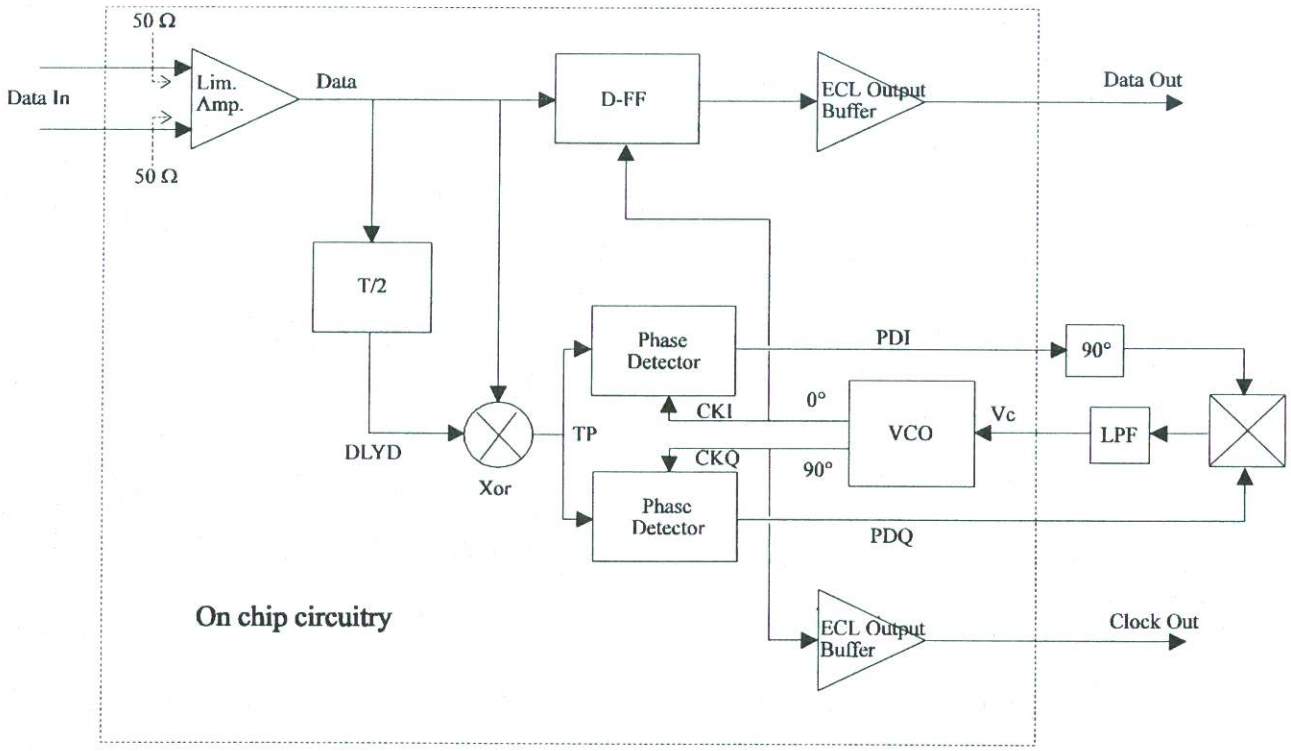

Fig. 1. Block scheme of the clock and data recovery circuit.

To obtain the required output dynamic range of 400 mVpp single ended is necessary to concentrate the gain on the first differential stage, using the second one mainly as a limiting block; the two stages differential voltage gains are 16 dB and 9 dB respectively. We have chosen to obtain these gains using large channel widths for the driver transistors, more than biasing them to have a high specific transconductance g_{mo}. This permits to have high differential gains ($Ad = g_{mo} * W * R_L$, where W is the channel width of the driver transistor and R_L is the load resistance) even with a limited dynamic output range ($2 * W * R_L * I_{dso}$, where I_{dso} is the channel current per unit width), exploiting a particular feature of the IAF HEMT's, which present a sufficiently high value of g_{mo} even when biased with very low I_{dso}. The simulated performance of the limiting amplifier is listed in Tab. 1.

Differential Voltage Gain	25 dB
3 dB Bandwidth	7.7 GHz
Output dynamic range	400 mVpp s.e.
Linear input range	30 mVpp s.e.
Power dissipation	90 mW
Low freq. cut-off	100 KHz

Tab. 1. Limiting amplifier characteristics.

Clock recovery circuit - The clock recovery circuit is formed by a delay line/EX-OR pulse generator followed by a F/PLL loop based on the Richman's quadricorrelator. The frequency acquisition loop requires two high speed phase detectors and a VCO with in-phase and in-quadrature outputs. The phase detector outputs are combined using low-frequency external circuitry (90° phase shifter, frequency difference detector, low pass filter) to obtain the error signal proportional to the frequency difference. The half-bit delay line has been implemented using a microstrip stub [2], placed on the alumina substrate which houses the chip and the bias networks. Figure 2 shows the principle of the delay line, based on the delay properties of a shorted transmission line stub.

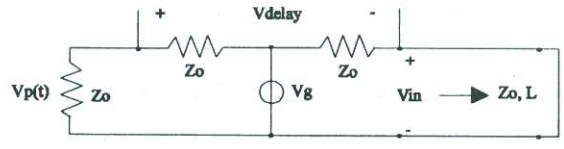

Fig. 2. Microstrip stub delay line principle.

A pulse Vg(t) is launched onto this line stub by a signal source whose internal impedance equals the line characteristic impedance Zo. At the shorted end of the line the pulse is reflected back to the source and returns to the source terminals undistorted, but with a negative sign and delayed by twice the electrical length of the line. So we have $Vin(t) = Vp(t) - Vp(t-2\tau)$, where $Vp = Vg/2$, and using a voltage splitter to obtain a copy of Vp(t) we have $Vdelay = Vp(t) - Vin(t) = Vp(t-2\tau)$. The VCO has been implemented using the differential topology shown in figure 3, where the external passive components have to be chosen to reduce the frequency offset between the bit-rate and the VCO free-running frequency. The VCO is based on the multivibrator topology and is completely balanced, which not only prevents injection locking, but also helps to reduce upconversion of 1/f noise.

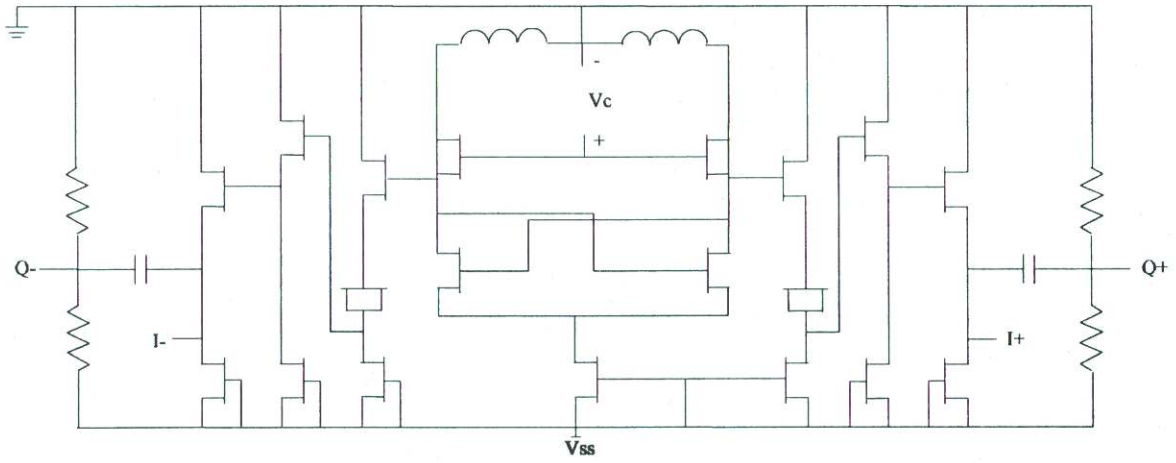

Fig. 3. Voltage controlled oscillator.

Decision circuit - The decision element has been designed as a D-type Master-Slave flip-flop, composed of two identical latches, formed by two differential cells connected in a positive feedback configuration whose bias currents are switched by the clock signal. When a clock transition switches off the first cell, the second one is forced into saturation by the positive feedback, latching the data. The cross-connection of the clock signal to the current switching cells of the two latches provides the master-slave operation of the flip-flop. The simulated performance of the flip-flop is listed in Tab. 2.

Set up time	15 psec
Hold time	0
Tr, Tf	50 psec

Tab. 2. Master slave flip-flop simulated performance.

3. Measurement results - Figure 4 shows a microphotograph of the chip, which measures 2x2 mm.

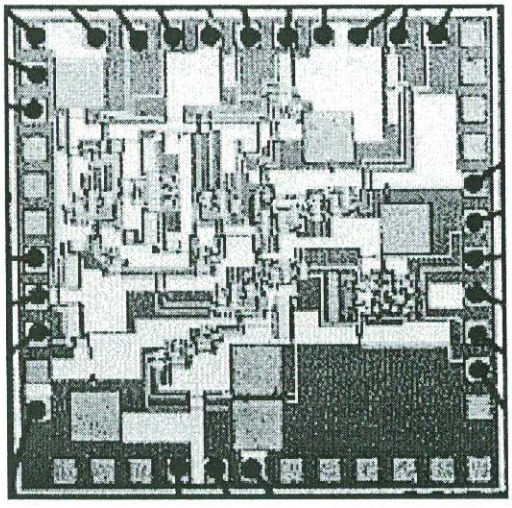

Fig. 4. Photomicrograph of the 2.5 Gb/s Clock Recovery and Data Regenerator die.

Two chips have been placed in a LCC Kyocera ceramic package with a 6x6 mm die-cavity. The package contains also Murata blocking capacitors for the DC feedback loop of the limiting amplifier. The chips have been tested using a PCB circuit with the low-frequency biasing networks and the external VCO passive components. The measured performance is in good agreement with the simulations and is summarised in Tab. 3.

Input sensitivity	30 mVpp
Output jitter	10 psec rms
Power consumption	1.3 W

Tab. 3. Clock and data recovery circuit measured characteristics.

In figure 5 are shown the output eye-diagram and the recovered clock signal with a NRZ 2^{15}-1 PRBS. The estimated rise and fall time is 150 psec, and the rms clock jitter is about 10 psec.

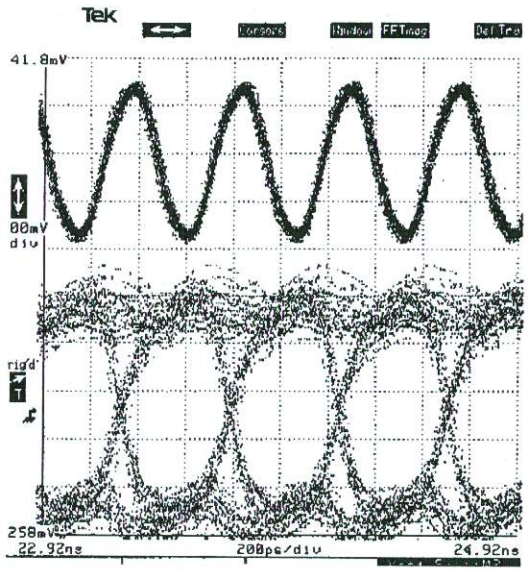

Fig. 5. Recovered Clock (VCO output) and Regenerated Data (Flip/Flop Output) with a 2^{15}-1 pseudo-random NRZ data stream.

4. Conclusion - A monolithic GaAs clock and data recovery circuit has been designed and tested using IAF FhG HEMT technology. The fabricated chip comprises analog and digital functions and uses about 200 active devices. Sample chips have been packaged using a ceramic package and have been tested by using BER test equipment. The results of the measurements are in a good agreement with the expected ones, except for what concerns the input sensitivity which is lower than the expected one by 3dB. This can be due to crosstalk in the package owing to the lenght of the bonding wire and will be checked by measurements we are going to do using MIC bonding scheme and alumina substrate.

References

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