A W-band MMIC amplifier using 70-nm gate length InP HEMT technology

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Abstract — InP HEMT transistors using 70-nm gate length have been fabricated and modeled. Two different epitaxial structures have been tested based on either single- or composite InGaAs channel. The composite-channel HEMT exhibited significantly higher maximum transconductance, 1370 mS/mm, compared to 860 mS/mm for the single-channel HEMT whereas \( f_t \) (\( f_{\text{max}} \)) was approximately the same, 190 (260) GHz, and 200 (320) GHz, respectively. A W-band microstrip MMIC amplifier using 70-nm gate length InP HEMT technology has been designed and fabricated for the single-channel structure. The one-stage amplifier exhibited a gain of 8 dB at 94 GHz.

I. INTRODUCTION

InGaAs-InAlAs-InP HEMT technology is the preferred choice for circuit applications targeting low noise at mm-wave frequencies. However, the optimization of a sub-100 nm technology is very sensitive to a number of parameters in the epitaxial structure [1]. We here report issues of design, fabrication and modeling of 70-nm gate length InP HEMTs using either a single or a composite structure in the active channel. The single-channel design has been implemented in a microstrip-based process. A one-stage W-band MMIC amplifier is demonstrated.

II. HEMT STRUCTURES

The layers of the two different HEMT structures were grown by molecular beam epitaxy (MBE) on a Fe-doped semi-insulating InP substrate. The composite channel contains an InGaAs super-lattice structure with five periods of four-to-one monolayers InAs/GaAs resulting in an effective composition of 80% In. The gate-to-channel distance is 115 Å for the single-channel and 140 Å for the composite-channel. Details for the different layers are given in Fig. 1.

III. DEVICE PERFORMANCE

Details of the processing flow of the transistors are described in Ref. [2]. A scanning-electron microscope (SEM) image of a device is shown in Fig. 2. The DC current-voltage (I-V) characteristics of passivated 2x35 \( \mu \)m devices were measured on-wafer, see Fig. 3. The thickness of the Schottky barrier for the single-channel material was probably too low hence explaining the suppression of the drain current \( I_d \). The pinch-off characteristic is well-behaved for both devices. The measured extrinsic transconductance \( g_{m} \) is shown in Fig. 4. A maximum \( g_{m} \) of 860 mS/mm and 1370 mS/mm is obtained for the single- and composite-channel design, respectively, at a \( V_{ds} \) of 1.0 V. The difference in \( g_{m} \) between the two channel design seen in Fig. 4 is connected to the difference in the electron mobility \( \mu_e \) and sheet carrier concentration \( n_s \) for the two HEMT structures; The measured \( \mu_e \times n_s \) is more than 50% larger for the composite-channel compared to the single channel design.

The s-parameters of the devices were measured on-wafer up to 50 GHz using coplanar probes and a HP8510

Fig. 1. Epitaxial InP HEMT structure for (a) single-channel and (b) composite-channel design.
Fig. 2. A SEM image of a 70-nm InP HEMT with a gate width of 2x35 µm.

vector network analyzer. A -20 dB/decade extrapolation of current gain \(|h_{21}|^2\) and Mason’s gain \(U\) versus frequency using least square fits gives an extrinsic \(f_t\) and \(f_{\text{max}}\) of 200 GHz and 320 GHz, respectively for the single-channel HEMT. For the composite design, \(f_t\) was extrapolated to 190 GHz and \(f_{\text{max}}\) to 260 GHz, see Fig. 5. Despite the large difference in \(g_m\) between the two HEMTs, the \(f_t\) and \(f_{\text{max}}\) numbers are approximately the same. This is explained by the higher output conductance for the composite-channel design. In other words, \(g_m/g_d\) is similar for the two HEMTs as verified by extracted device small-signal model parameters.

IV. DEVICE MODELING

The devices have been modeled by a direct extraction method and optimized using a sequential optimization method [3]. In Fig. 6, the small signal model used for these InP HEMT devices is shown. A normalized error analysis of the model has been performed over 168 different bias points. The normalized error function \(\varepsilon\) is defined as:

\[
\varepsilon = \frac{1}{4N} \sum_{j=1}^{2} \sum_{k=1}^{\text{max}\{\text{meas}\}} \frac{1}{\sqrt{\text{meas}}(k) - S_{ij}^{\text{model}}(k)}^2
\]
In Fig. 7 the normalized errors for the different materials are plotted versus $V_{ds}$ and $V_{gs}$. The models exhibit a good fit over a large range of bias points and can therefore be used for large signal modeling. The error increases at higher $V_{ds}$ due to impact ionization [4], which is not accounted for in the model. The variation in normalized error for the composite-channel is correlated to the bias dependence of $g_m$.

Fig. 8 shows the measured and modeled s-parameters at $V_{ds}$=1.1 V between 1 GHz and 50 GHz. Apart from lower frequencies below 5 GHz, the agreement is excellent for all s-parameters. To achieve a better fit with the measured data at low frequencies, the model must include a part which describes impact ionization.

V. MMIC PERFORMANCE

The W-band amplifier was designed using 2x35 µm InP HEMT single-channel devices. The agreement between the applied small-signal model and measured data is represented in Fig. 8(a). The model is extrapolated to W-band. The s-parameters of the amplifier were measured with a W-band test set using an on-chip TRL calibration. The transistor was biased through bias Tees. As depicted in Fig. 9, the amplifier exhibited more than 8 dB gain over 75-94 GHz.
We have investigated two different 70-nm gate length InP HEMTs based on either single- or composite InGaAs channel design. A W-band microstrip amplifier has been fabricated and characterized for the single-channel 70-nm InP HEMT. The amplifier exhibited more than 8 dB gain from 75 to 94 GHz.

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**REFERENCES**


