# RF Characteristics of BJT Devices with Selectively or Fully Ion-Implanted Collector

C. C. Meng<sup>1</sup>, J. Y. Su<sup>1</sup>, B. C. Tsou<sup>2</sup> and G. W. Huang<sup>3</sup>

<sup>1</sup>National Chiao Tung University, Department of Communication Engineering, Hsin-Chu 300, Taiwan, R.O.C.

email:ccmeng@mail.nctu.edu.tw, Tel:886-3-5131379, Fax:886-3-5736952 <sup>2</sup> National Chung-Hsing University, Department of Electrical Engineering, Taichung 400, Taiwan, R.O.C.

<sup>3</sup> National Nano Device Laboratories, Hsin-Chu 300, Taiwan, R.O.C.

*Abstract* — A selectively ion-implanted collector (SIC) is implemented in a 0.8 um BiCMOS process to improve the RF characteristics of the BJT devices. The SIC BJT device has better ft and fmax than the FIC (fully ion-implanted collector) BJT device because the extrinsic base-collector capacitance is reduced by the SIC process. The fmax is 9.5GHz and ft is 7.8 GHz for the SIC BJT device while the fmax is 7.2 GHz and fmax is 4.5 GHz for the FIC BJT device when biased at Vce=3.6 V and Jc=0.09 mA/um<sup>2</sup>. The nois parameters are the same for both BJT devices but the associated gain is higher for the SIC BJT device.

#### I. INTRODUCTION

The selectively ion-implanted collector can reduce the extrinsic base-collector junction capacitor and thus improve the BJT circuit speed. The collector ion-implantation can confine the base profile layer by compensating the base profile tail due to channeling effect. The base width with an SIC can be reduced by a factor of 1.5 by applying this technique and thus the speed can be improved by about 2 times [1]. The SIC can also improve the d.c. current gain and suppress the base push-out effect. Thus, the speed of the BJT device can be improved by operating the device at higher current. In this paper, the effects of the selectively ion-implanted collector on the rf characteristics are analyzed. The cross sectional view of the SIC BJT device and FIC BJT device are shown in Fig. 1(a) and Fig. 1(b), respectively. Two BJT devices fabricated on the same wafer in the adjacent area are compared. The SIC BJT device has the selectively ion-implanted collector only underneath the emitter area while the FIC BJT device has the ion implanted collector over the whole base area. In other words, the two devices have the same intrinsic region but the SIC BJT has the less extrinsic base-collector capacitance. Here, we are not comparing two devices with the selectively ion-implanted collector and without the selectively ion-implanted collector. A SIC BJT device has different dc characteristics from a BJT device without the ion-implanted collector because the base layer is narrowed by the collector ion implantation and the

intrinsic collector has different doping density. However, the d.c. characteristics for the SIC and FIC BJT devices are identical because the intrinsic regions of both devices are the same. Thus, it sets a fair background to probe the effects of the extrinsic base-collector region to the device rf characteristics.

## II. DEVICE STRUCTURE AND DC CHARACTERSITICS

The BJT device here has 0.8 um emitter width, 6 um emitter length, and 20 emitter fingers. The I-V curves of the SIC and FIC BJT devices are shown in Fig. 2. Both devices have very close common-emitter I-V curves. The device has  $\beta$  of 160 and BVCEO of 9 V. The forward Gummel plot and reverse Gummel plot of both BJT devices are identical and are shown in Fig. 3. The BJT device has the desired 1 kT base current for the range of more than six orders of magnitude. The diode I-V curves of both BJT devices when the emitter is open are also shown in Fig. 4 and the both BJT devices have almost equal open-emitter breakdown voltage. The emitter fingers are interleaved with the base fingers to reduce the base resistance. The base contact width is 1 um. It is a non-self-aligned BJT process and the spacing between the emitter edge and base edge is 2.3 um. There is no extra cost for this SIC structure because the SIC process is merged with the anti-punch-through ion implantation in the subsurface region for the buried channel PMOS device in the 0.8 um BiCMOS process. The mask opening for the collector ion-implantation is the same size as the emitter area for the SIC BJT device and the same size as the base area for the FIC BJT device, respectively.

## **III. RF CHARACTERISTICS**

S parameters were measured up to 20 GHz for both BJT devices. GS pads instead GSG pads are designed with the  $0.8X6X20 \text{ um}^2$  BJT device to reduce the pad parasitic effects. The measured ft and fmax for Vce=3.6 V are shown in Fig. 5. The SIC process almost does not change

ft but improves fmax significantly. The emitter-collector charging time ( $\tau_{ec}$ ) is the reciprocal of the cut-off radian frequency and is decomposed into emitter charging time ( $\tau_e$ ), base transit time ( $\tau_B$ ), base-collector transit time( $\tau_C$ ) and collector charging time ( $\tau_C$ ) as follows [2].

$$\tau_{\rm EC} = \frac{1}{2\pi f_{\rm T}} = \tau_{\rm E} + \tau_{\rm B} + \tau_{\rm C} + \tau_{\rm C} \,' \tag{1}$$
$$\tau_{\rm C} \,' = (R_{\rm E} + R_{\rm C})C_{\rm jC} \tag{2}$$

Where  $C_{jC}$ ,  $R_E$  and  $R_C$  are the base-collector capacitance, emitter static resistance and collector static resistance, respectively. The major difference between two BJT devices is the collector charging time and the collector charging time is insignificant when compared to other time constants. Normally, the base transit time is the dominant time constant. Thus, two BJT devices are expected to have very close ft as shown in Fig. 5. The fmax can be related to the ft by the following formula.

$$f_{max} = \sqrt{\frac{f_t}{8\pi r_{bb}C_{jC}}}$$
(3)

Where, rbb is the base access resistance and is almost the same for both BJT devices. Thus, the factor of 2 improvement in fmax for the SIC BJT device mainly comes from the reduction of the extrinsic base-collector junction capacitance. The extrinsic base access resistance is slightly smaller for the SIC BJT device. The fmax is 9.5 GHz and ft is 7.8 GHz for the SIC BJT device while the fmax is 7.2 GHz and fmax is 4.5 GHz for the FIC BJT device when biased at Vce=3.6 V and Jc=0.07 mA/um<sup>2</sup>.

Noise parameters for the two BJT devices were measured by the commercial source-pull noise measurement system by ATN. NFmin, Rn, and Yopt constitute the noise parameters. Here, Fmin is the minimum noise figure, Rn is the noise resistance, and Yopt(=Gopt+jBopt) delegates the optimal source admittance for the minimum noise figure. The NFmin, Rn, and associated gain as a function of frequencies are shown in Fig. 6. The optimal source conductance (Gopt) and susceptance (Bopt) for the minimum noise figure as a function of frequency is shown in Fig. 7. It can be seen from Fig. 6 and Fig. 7 that the noise parameters are almost the same for both devices except that the SIC BJT device has a 1.5 dB higher associated gain. The noise resistance is a constant for different frequency, the optimum source conductance and the optimum source susceptance are proportional to frequency. The minimum noise figure increases for higher frequencies. The dependence of the noise parameters of a BJT device can be written as follows [3].

$$R_{n} = \frac{V_{t}}{2I_{C}} + (r_{E} + r_{B})$$
(4)  

$$Y_{sop} = \frac{f}{f_{t}R_{n}} \left\{ \sqrt{\frac{I_{C}}{2V_{t}} (r_{E} + r_{B}) \left(1 + \frac{f_{t}^{2}}{\beta_{0}f^{2}}\right) + \frac{f_{t}^{2}}{4\beta_{0}f^{2}}} - j\frac{1}{2} \right\}$$
(5)  

$$F_{MIN} = 1 + \frac{1}{\beta_{0}} + \frac{f}{f_{t}} \sqrt{\frac{2I_{C}}{V_{t}} (r_{E} + r_{B}) \left(1 + \frac{f_{t}^{2}}{\beta_{0}f^{2}}\right) + \frac{f_{t}^{2}}{\beta_{0}f^{2}}}$$
(6)

Both BJT devices have similar noise parameter because of the small difference in ft. Here,  $\beta_0$  is the dc current gain. The noise resistance is not a function of frequency from equation (4). The frequency of Gopt and Bopt from equation (5) is complicated. However, a corner frequency f<sub>a</sub> for noise can be defined as follows.

$$f_a = \frac{f_t}{\sqrt{\beta_0}}$$
(7)

Thus, the formula for Yopt can be simplified.

$$Y_{sop} = \frac{1}{R_{n}} \left\{ \sqrt{\frac{I_{C}}{2V_{t}} (r_{E} + r_{B}) \frac{1}{\beta_{0}} + \frac{1}{4\beta_{0}}} - j\frac{1}{2}\frac{f}{f_{t}} \right\} \text{ for } f < f_{a} \quad (8)$$

$$Y_{sop} = \frac{f}{f_{t}R_{n}} \left\{ \sqrt{\frac{I_{C}}{2V_{t}} (r_{E} + r_{B}) + \frac{f_{t}^{2}}{4\beta_{0}f^{2}}} - j\frac{1}{2} \right\} \text{ for } f > f_{a} \quad (9)$$

The d.c. current gain is 160 and ft is about 7 GHz. Thus, the noise corner frequency is about 0.6 GHz and is below the measured frequency. Thus, eqn (9) applies and both the optimal source conductance and susceptance are proportional to frequency as shown in fig. 7. The concept of the noise corner frequency is also valid for the Fmin. Here, we have

$$F_{MIN} = 1 + \frac{1}{\beta_0} + \sqrt{\left(\frac{2I_C}{V_t} \left(r_E + r_B\right) + 1\right) \frac{1}{\beta_0}} \qquad \text{for} \quad f < f_a$$
(10)

$$F_{\min} = 1 + \frac{1}{\beta_0} + \sqrt{\frac{2I_C}{V_T} (r_E + r_B) \frac{f^2}{f_T^2} + \frac{1}{\beta_0}} \qquad \text{for} \quad f > f_a$$
(11)

Thus, the minimum noise figure increases in Fig. 6 as expected.

### VI. CONCLUSION

The SIC process improves fmax because the reduction of the extrinsic base-collector capacitance. A noise corner frequency is introduced for the BJT device to describe the frequency dependence of the noise parameters. Both BJT devices have similar noise parameter because of the small difference in ft but the associated gain is higher for the SIC BJT device. There is no extra cost for this SIC structure because the SIC process is merged with the antipunch- through ion-implantation in the subsurface region for the buried channel PMOS device in the 0.8 um BiCMOS process.

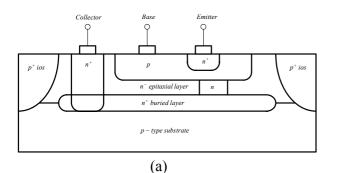
#### REFERENCES

[1] S. Konaka, E. Yamamoto, K. Sakuma, Y. Amemiya and T. Sakai, "A 20-ps Si bipolar IC using advanced super selfaligned process technology with collector ion

implantation," IEEE trans.on electron devices, vol. 36, no.7, pp.1370-1375, July 1989.

[2] M. Kahn, S. Blayac, M. Riet, P. Berdaguer, V. Dhalluin, F. Alexandre, and J. Godin, "Measurement of base and collector transit times in thin-base InGaAs/InP HBT," *IEEE Electron Device Letters*, Vol. 24, NO. 7, pp. 430-432, July 2003.
[3] S. P. Voinigescu et al., "A scalable high-frequency noise

[3] S. P. Voinigescu et al., "A scalable high-frequency noise model for bipolar transistors with application to optimal transistor sizing for low-noise amplifier design," *IEEE journal of solid-state circuits*, Vol. 32, No. 9, pp.1430-1439, Sep. 1997.



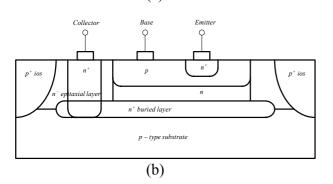


Fig. 1. Structures for the (a) SIC BJT devices (b) FIC BJT devices.

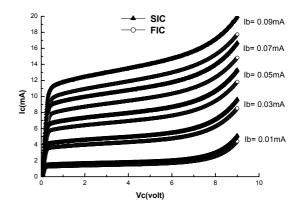


Fig. 2. Common-emitter I-V curves of the SIC and FIC BJT devices.

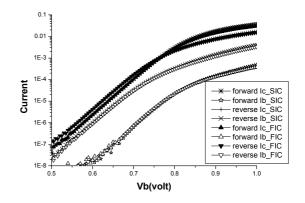


Fig. 3. Forward and reverse Gummel plot of the SIC and FIC BJT devices.

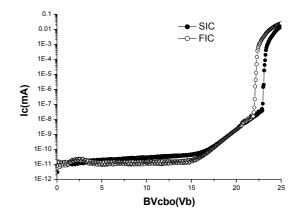


Fig. 4. Open-emitter base-collector diode I-V curves of the SIC and FIC BJT devices when the base-collector junction is reverse-biased.

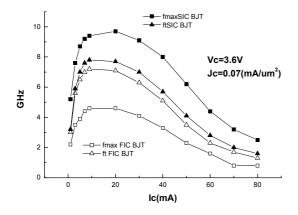


Fig. 5 ft and fmax of the SIC BJT device and FIC BJT device at Vce=3.6 V Jc=0.07 mA/um<sup>2</sup>.

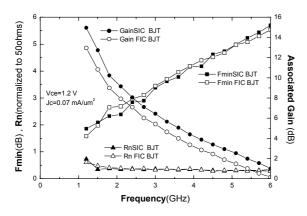


Fig. 6 NFmin, Rn, and associated gain of the SIC BJT device and FIC BJT device at Vce=1.2 V and Jc=0.07 mA/um<sup>2</sup>.

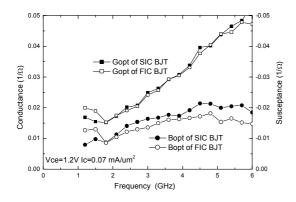


Fig. 7 Gopt and Bopt of the SIC BJT device and FIC BJTdevice at Vce=1.2 V and Jc=0.07mA/um<sup>2</sup>.