A 2 GHz CMOS dB-Linear Programmable-Gain Amplifier with 51 dB Dynamic Range

L. Wu[1)], U. Basaran[1)], R. Tao[1)], M. Berroth[1)], Z. Boos[2)]

[1)]Institute of Electrical and Optical Communication Engineering, University of Stuttgart, Germany
Pfaffenwaldring 47, D-70550 Stuttgart, Germany
Tel: 49 711 685-7899 Fax: 49 711 6857900
Email: wu@int.uni-stuttgart.de Web: http://www.uni-stuttgart.de.int
[2)]Infineon Technologies AG, Kastenbauerstr. 2, D-81677 Munich, Germany

***Abstract* — A 2 GHz programmable-gain amplifier (PGA) using 0.12-µm CMOS technology is presented in this paper, which has a 51 dB gain control range with 3 dB gain control steps. The maximum output power of this PGA achieves 9 dBm while the 1-dB compression point is located at 8 dBm. A high linearity denoted by the oIP3 of 22 dBm at the maximum gain has been achieved. A new configuration to digitally implement a dB-linear gain characteristic is demonstrated in this paper, which simultaneously enables an adaptive power consumption.**

I. INTRODUCTION

Programmable-gain amplifiers have become an indispensable function block for many mobile communication systems in order to maximize the overall system dynamic range. In code-division multiple access (CDMA) systems, for instance, the mobile transmitter is required to provide at least 80 dB of the dynamic gain control range [1]-[3]. Normally, it is realized by an intermediate frequency (IF) stage and a radio frequency (RF) stage. In this paper, we propose a radio frequency PGA, which is fabricated using a standard 0.12 µm CMOS technology.

CMOS is the technology of choice for a higher integration level and lower cost because it is capable of implementing a significant amount of digital signal processing and because the vast majority of today´s integrated circuits are implemented in this technology. However, for a CMOS technology, it is difficult to make an exponential or logarithmic function because the normal operation of an MOS transistor shows a square-law transfer characteristic. Therefore, a linear-in-dB gain variation implemented in a CMOS technology can only be fulfilled, using an approximate rational function instead of an exponential function [4]. However, the maximum gain control range obtained in this way is limited within 30 dB. For an even larger gain range, parasitic bipolar transistors can be used for accurate exponential transformation [5]. It has also been attempted to develop a PGA for a large dynamic gain range with linear-in-dB gain variation simply in a CMOS technology, several cascaded PGA stages have been used [6].

In this paper, a new configuration for a PGA design is introduced. Eighteen individual amplifier cells designed for 18 different voltage gain steps are connected in parallel and are digitally controlled by a 5 to 18 demultiplexer, resulting in a gain control range between 8 dB and -43 dB with 3 dB gain control steps. To the best of the authors´ knowledge, this 51 dB gain variation is the largest gain control range reported so far for a radio frequency PGA. A PGA has normally discrete gain variation causing indeed phase discontinuity, however, the amount of it is well below what is currently specified in the 3GPP UMTS specifications. Therefore, it is not critical to use a PGA in UMTS transmitter applications. Operating at 2 GHz, this PGA can directly be used as the PA driver for cellular applications. With a supply voltage of 2.5 V, the maximum output power reaches 9 dBm, while the 1-dB compression point is located at 8 dBm. The output third order intercept point (oIP3) is as high as 22 dBm. Compared with an IF PGA design, much more DC power consumption is an essential problem suffered by the RF PGA design. To save battery power, an adaptive current consumption has been designed in our work, which reduces the DC current flowing through the circuit when the PGA operates with a lower gain.

Section II describes the circuit and implementation details. In Section III, experimental results are presented. These are followed in Section IV by the conclusions drawn from this work.

II. CIRCUIT DESCRIPTION

The block diagram of the PGA is illustrated in Fig. 1. In order to obtain a dynamic gain range of 51 dB with 3 dB gain control steps, this circuit employs 18 parallel amplifier cells for different gains. V_{DD} and V_{dd} are power supplies used for the amplifier cells and the demultiplexer, respectively. The gain of an MOS amplifier depends on the transconductance g_m, which is approximately proportional to the gate width. Therefore, devices with different gate width are selected for different amplifier cells according to the 3 dB gain difference. At any given time, only one amplifier cell is turned on. Therefore, linear-in-dB gain and 3 dB gain steps can be easily obtained in this manner. Since the bias current flowing through the devices is also proportional to the gate width, the adaptive DC current consumption can be automatically fulfilled with this configuration of parallel connected amplifier cells. On the other hand, more parallel amplifier cells require naturally more chip area, however, since the most amplifier cells are designed for attenuation, devices with only very small dimensions are used in these cells. Especially, the LC

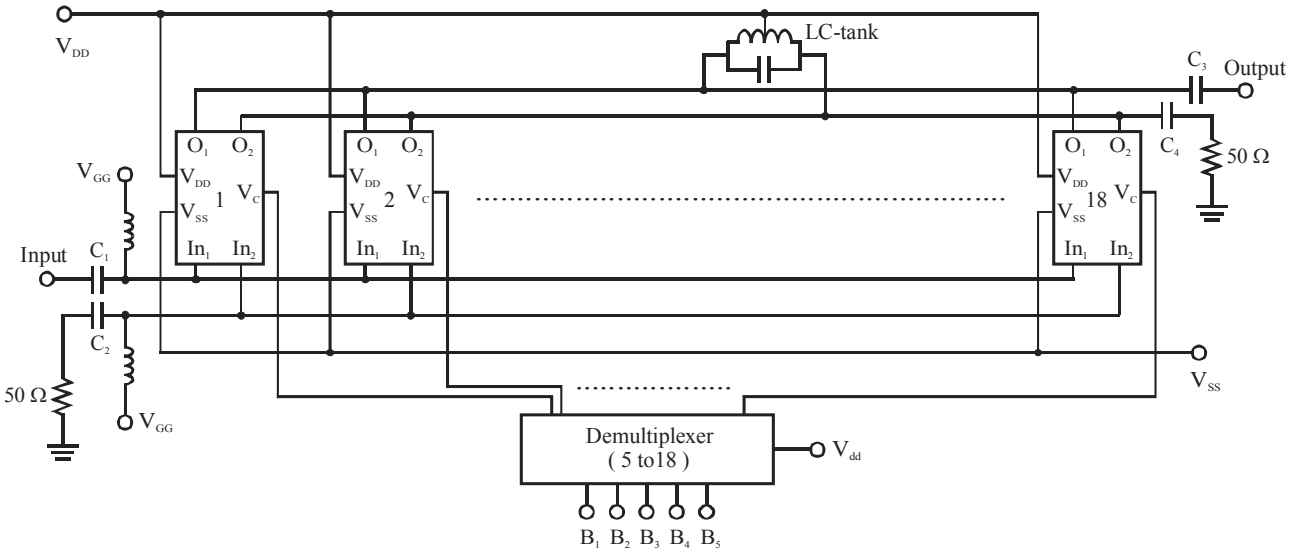

Fig. 1. Block diagram of the proposed PGA.

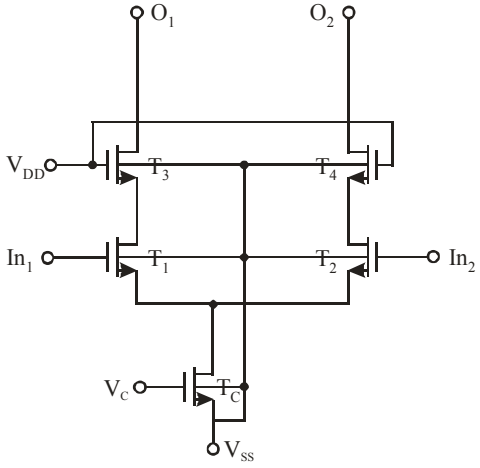

Fig. 2. Schematic of an amplifier cell.

tank shown in Fig. 1, which is also integrated on the chip, is used as the common load for all the parallel amplifier cells. Compared with the chip area occupied by the inductor and the capacitor, the chip area invested for the most attenuation cells are really as small as negligible. This LC tank is tuned to have a resonance frequency of 2 GHz. Compared with resistive loads or MOS loads, a LC tank consumes no voltage headroom. Therefore, a larger output voltage swing can be obtained generating a higher output power.

Normally, a PGA is applied in a feedback loop to form an automatic-gain control (AGC). The PGA is implemented in an analog radio frequency transceiver integrated circuit (IC) while the rest of the AGC is realized in a digital base-band modem (modulator/demodulator) IC. In this work, a 5 to 18 demultiplexer, which is also integrated on the chip, is used to control all the amplifier cells. Its output digital control words are defined as 1 to 18 implying the increasing gain. B_1 – B_5 shown in Fig. 1 indicate the 5 demultiplexer input bits which are used as the digital interface to the outside.

Fig. 2 presents the schematic of a single amplifier cell. To obtain the higher immunity to noise and crosstalk coming from substrate and power supply, differential circuits are proposed for all the amplifier cells. Cascode stages are used in the differential pairs to minimise the Miller effect. Guard rings are employed around the devices to reduce the substrate noise. Gate width of the devices T_1 – T_4 are determined according to the voltage gain expected from each cell. Device T_C is used as a current source of the differential pair, whose gate is connected to one of the eighteen outputs of the demultiplexer. Therefore, this cell is activated as soon as the connected demultiplexer output has a high voltage level. The demultiplexer is naturally so designed that only one output has a high voltage level at any given time. Single ended input and output are expected from this PGA, therefore, the input In_2 of each amplifier cell is connected with a 50 Ohm (the reference impedance) resistor through the input AC coupling C_2, whereas the output O_2 of each amplifier cell is also connected with a 50 Ohm resistor through the output AC coupling C_4 as shown in Fig. 1.

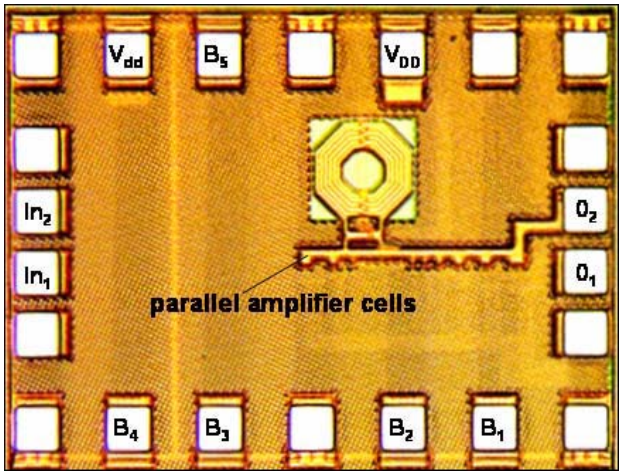

Fig. 3. Micrograph of the PGA chip.

III. Measurement Results

A PGA test chip was fabricated in a standard 0.12-µm CMOS technology. A micrograph of this chip is shown in Fig. 3. The parallel amplifier cells can be seen using a relative small chip area. The whole active area occupies 0.5 x 0.4 mm^2. The supply voltage are 2.5 V for the amplifier cells and 1.5 V for the demultiplexer, respectively. The 5 to 18 demultiplexer is also integrated on the chip, which only uses a very small chip area. The pads B_1 – B_5 shown in Fig. 3 indicate the five demultiplexer inputs.

Fig. 4 shows the measured voltage gain versus the digital gain control words at 2 GHz. The gain can be varied from -43 dB to 8 dB with a control step of about 3 dB. A gain control range of 51 dB has been achieved. This result implies that this techniques is effective for a PGA design. Theoretically, a even larger dynamic range can also be realized in this way. However, an attenuation state can sometimes be limited at a high frequency due to the direct coupling between the input und output of the circuit through the silicon substrate.

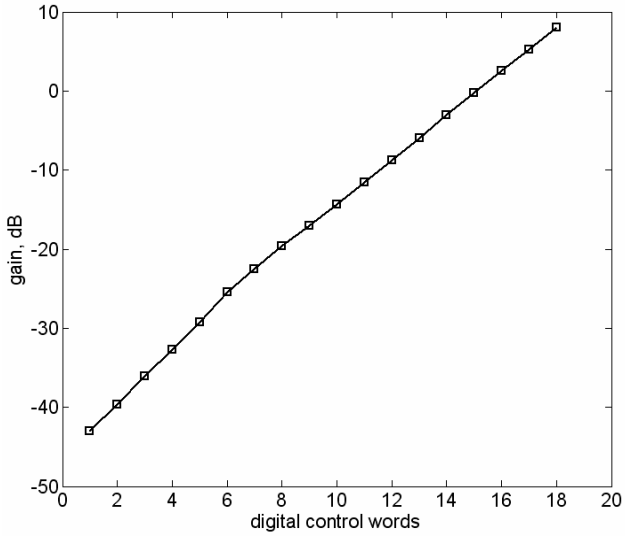

Fig. 4. The gain versus digital control words at 2 GHz.

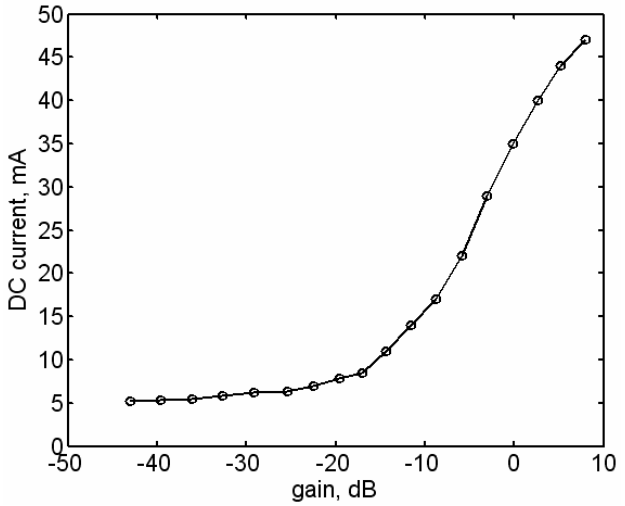

Fig. 5. DC current consumption versus the voltage gains at 2 GHz.

The measured DC current versus the voltage gain is presented in Fig. 5. Obviously, it can be reduced with a lower voltage gain. Adaptive power consumption has been obtained. Since all the amplifier cells have the same load, the PGA has nearly a constant bandwidth while the gain changes. The frequency response of the PGA is shown in Fig. 6, which is measured with the gain of -4 dB at 2 GHz. A 3-dB bandwidth of 700 MHz has been obtained. Fig. 7 shows the input-referred output power and the oIP3 at 2 GHz measured with the maximum gain. The maximum output power reaches 9 dBm, while the 1-dB compression point is located at 8 dBm. The oIP3 is as high as 22 dBm. The measured results of the third-order and fifth-order intermodulation distortion (IMD3 and IMD5) have been shown in Fig. 8, as a function of the PGA output power. IMD3 better than -40 dBc has been accomplished when the PGA output power is lower than about 3 dBm. However, it can be degraded if the output power increases. Compared with an IF PGA, this is a typical critical feature of an RF PGA. Therefore, An RF PGA or VGA should normally be linearized using a predistorter [7].

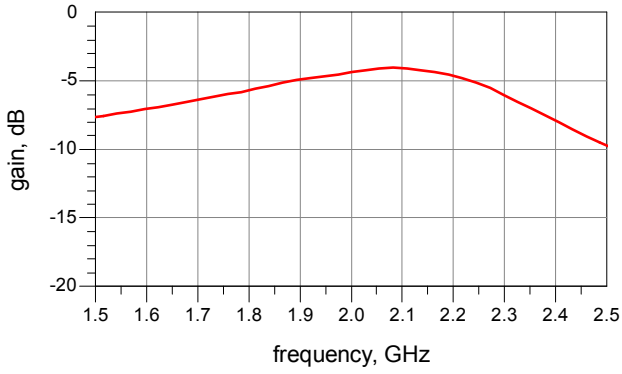

Fig. 6. Measured frequency response of the PGA with the gain of -4 dB at 2 GHz.

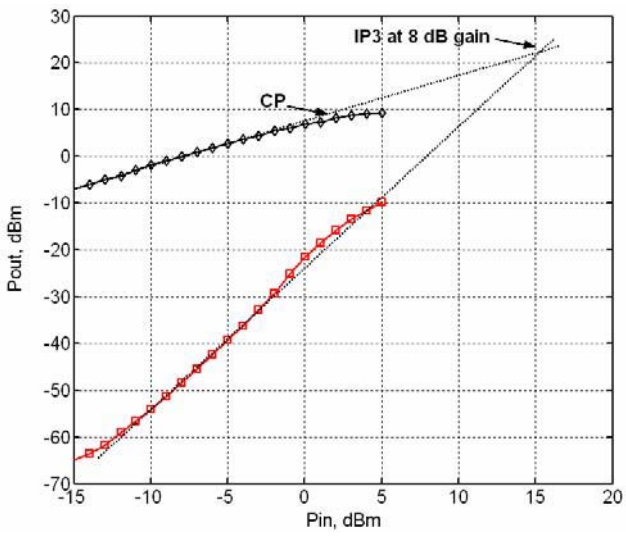

Fig. 7. Measured output power and IP3 versus the input power at 2 GHz.

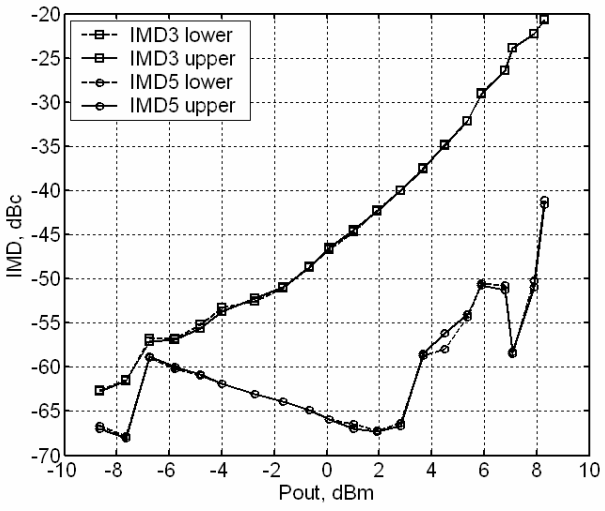

Fig. 8. Measured IMD at 2 GHz.

IV. CONCLUSION

An RF PGA operating at 2 GHz has been designed and fabricated using a standard 0.12 µm CMOS technology. A large gain control range, adaptive power consumption, broad bandwidth and high linearity at RF have been achieved. A novel configuration for a PGA design with linear-in-dB gain variation has been presented, which could be applied to many other device technologies.

REFERENCES

[1] Recommended Minimum Performance Standards for CDMA2000 Spread Spectrum Mobile Station, 3GPP2 Doc. C.S0011-A

[2] Recommended Minimum Performance Standards for Dual-Mode Wide-band Spread Spectrum Cellular Mobile Station, IS-98A.

[3] Recommended Minimum Performance Standards for 1.8 to 2.0 GHz Code Division Multiple Access (CDMA) Personal Stations, ANSI J-Standard 018.

[4] R. Harjani, "A variable gain CMOS amplifier with exponential gain control," *in Symp. VLSI Circuits Dig. Tech. Papers,* June 2000, pp. 146-149.

[5] W. C. Song, C. J. Oh, G. H. Cho, and H. B. Jung, "High frequency/high dynamic range CMOS VGA," *Electron. Lett.,* vol. 36, pp. 1096-1098, Jun 2000.

[6] P. Orsatti, F. Piazza, Q. Huang, "A 71-MHz CMOS IF-baseband strip for GSM," *IEEE Journal of Solid-State Circuits,* vol. 35. No. 1, pp. 104-108, Jan. 2000.

[7] G. Hau, T. Nishimura, N. Iwata, "High efficiency, wide dynamic range variable gain and power amplifier MMICs for wide-band CDMA handsets," *IEEE Microwave and wireless components letters,* vol. 11. No. 1, pp. 13-15, Jan. 2001.