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An X-band GaAs MMIC down converter suitable for Doppler sensors

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Abstract. A $9.9 \div 10.7GHz$ down converter circuit, suitable for anti-burglar alarm systems, has been designed and realized in GaAs MMIC technology. The circuit transmits an RF signal towards a target and receives its frequency-shifted (Doppler effect) reflection, detecting possible movements of the target. In the paper a schematic description and details about the design methodology for the Dielectric Resonator oscillator and the Dual-FET mixer are given. Small and large signal measurements on the realized circuit are also presented.

Introduction

The down converter circuit (see the functional schematic in Fig.1) consists of a low noise local oscillator, a mixer and a suitable power splitting network. The signal provided by the local oscillator (at the frequency f_0) is split between the TX path and the LO input of the mixer. The latter provides an output IF signal detecting the Doppler frequency-shift of the received RF signal (at $f_s = |f_0 \pm f_d|$, f_d being the Doppler frequency-shift), reflected from a mobile target.

The main difficulties associated with the down-converter design are related to the presence of different nonlinear blocks which need suitable design procedures in order to meet the performance required taking also into account variations of the process parameters.

The series-feedback local oscillator is realized by a MESFET device and an "off-chip" coupled Dielectric Resonator (DR) for frequency stabilisation. The use of a Dielectric Resonator with high quality factor Q allows for good amplitude/frequency stability properties and low phase noise oscillation. Moreover, the operating frequency can be adjusted ($9.9 \div 10.7GHz$) through the selection of the DR and its placement with respect to the external coupling line, such that different national standards, concerning the operating frequency, can be met.

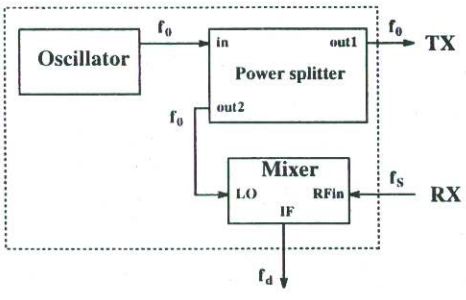

Fig.1: Functional schematic of the X-band down converter.

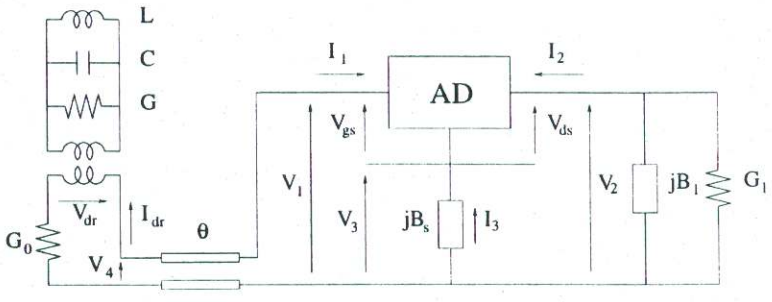

Fig.2: Equivalent diagram of the DR-stabilised oscillator.

System Design

A suitable design methodology for the series topology DR-stabilised oscillator has been developed[1]. Under the preliminary assumption of practically quasi-sinusoidal nonlinear operating conditions for the MESFET device and by selecting a suitable DC bias point [2], the following two-step procedure has been adopted. In the first step, assuming the "ideal" equivalent diagram in Fig.2 for the DR-stabilized oscillator, suitable phasors V_{gs}, V_{ds} of the RF operating voltages are searched for the maximum power

[1] The design methodology follows the same philosophy adopted in [1,2] for parallel feedback DROs.
[2] Eventually chosen by repeating the design procedure until the best performances are reached.

delivered from the device: $P_t = -Re[V_{ds}I_2^*]/2 - Re[V_{gs}I_1^*]/2$. In the "ideally lossless" conditions of Fig.2, this term can be also expressed as: $P_t = -Re[V_2I_2^*]/2 - Re[V_1I_1^*]/2 = P_{out} + P_{dr}$ where P_{out} is the power delivered to the load and P_{dr} accounts for dissipation on the Dielectric Resonator. If the losses in the DR are, as convenient, relatively small, P_t will therefore almost coincide with the RF output power.

The second step of the oscillator design methodology consists of a simple linear synthesis of the MESFET's passive (ideally lossless) feedback network, imposing self-starting conditions and maximising amplitude/frequency stability properties (as well as output power) [3]. In particular, specific stability indexes have been defined which enable to maximise the oscillator performance taking into account variations of the circuit parameters also due to process uncertainties. To this end, the circuit in Fig.2 can be conveniently studied at the connection port between the equivalent resonant circuit and the Active Non-Linear Bipole (ANB) composed by all the remaining circuit elements (including the MESFET and its biasing network). The stability analysis becomes quite simple if (with no relevant loss of accuracy owing to the necessarily high quality factor of the DR) the voltage V_{dr} is assumed to be practically sinusoidal. Under such conditions, a describing function approach can be adopted where the phasor I_{dr} of the current $i_{dr}(t)$ is expressed as a function of the amplitude $|V_{dr}|$ (zero phase can be assumed) of the almost sinusoidal voltage $v_{dr}(t)$: $I_{dr} = F(|V_{dr}|) = F_r(|V_{dr}|) + jF_i(|V_{dr}|) = |F|e^{j\phi}$ (where F_r, F_i, ϕ, are the real, imaginary part and phase of F, respectively).

Let $\widehat{f}$ and $|\widehat{V_{dr}}|$ be the frequency and the amplitude of the steady-state solution, then the stability properties of the DRO can be studied [1..3] in terms of the differential parameters: $g_0 = (dF_r/dV_{dr})_{V_{dr}=0}; g = (dF_r/dV_{dr})_{V_{dr}=\widehat{V_{dr}}}; b = (dF_i/dV_{dr})_{V_{dr}=\widehat{V_{dr}}}; \widehat{\phi} = arg[F(|\widehat{V_{dr}}|)]$, obtained by linearizing the non-linear characteristic $F[|V_{dr}|]$ at the steady-state solution $|\widehat{V_{dr}}|$ and at the initial solution $V_{dr} = 0$, respectively. In fact, under the hypothesis of a relatively large quality factor of the DR and denoting with G_{eq} the equivalent conductance accounting for the losses in the DR, it can be shown that the self-starting capability of the oscillator is guaranteed when the *small-signal instability factor* $K_i = g_0/G_{eq}$ is greater than one. Analogously, the steady-state solution is stable provided that the large-signal *amplitude stability factor* $K_a = g/G$ is smaller than one. Furthermore, in [3] it has been shown that a *frequency stabilization index* can be defined as: $K_f = |1/cos(\widehat{\phi})|\sqrt{1 + [(b/G_{eq} - tan(\widehat{\phi}))/(1 - g/G_{eq})]^2}$ such that the relative variation $\Delta f/\widehat{f}$ of the oscillation frequency, caused by any variation $\Delta F/\widehat{F}$ in the ANB characteristic (due to any possible perturbation in the MESFET, bias, load or feedback matching network), has an upper bound given by: $|\frac{\Delta f}{\widehat{f}}| \leq \frac{K_f}{2Q}|\frac{\Delta F}{\widehat{F}}|$.

For the series feedback oscillator of Fig.2, (provided that bias conditions and RF voltage amplitudes have been set), the stability indexes can be evaluated through a linearized analysis, as functions of the dissipated power on the Dielectric Resonator. In Fig.3 the stability indexes are shown as functions of the parameter [3] $\alpha_{dr} = P_{dr}/P_t$. The choice of α_{dr} univocally defines the values for the ideal components of the feedback network. In order to take into account "actual" foundry components and possibly non quasi-sinusoidal nonlinear conditions, a final optimisation of the circuit with commercially available Harmonic Balance tools is needed. This task takes advantage of the good first-guess estimation of circuit components obtained through the previous two step design procedure.

As far as the mixer design is concerned it has been realized through the Dual-FET configuration shown in Fig.4, which allows for good isolation properties between LO and RF ports without need for "size-consuming" filters or couplers. Moreover, an active FET mixer gives the possibility of conversion gain or, at least, of minor conversion losses. As well known [4], Dual-FET Mixers are based on the variations of the lower FET transconductance during each cycle of the LO signal applied to the upper FET Gate (V_{G2S1}). In Fig.4, the I_D current for the lower FET is plotted as a function of its Gate voltage V_{G1S1} with V_{G2S1} as parameter (simulation with foundry models). In order to have sufficiently large transconductance variations a bias voltage $V_{G1S1} = 0V$ has been adopted, allowing

[3] Denoting with α_{dr} the percentage of P_t dissipated on the DR ($P_{dr} = \alpha_{DR}P_t$), then the output RF power can be simply expressed as: $P_{out} = (1 - \alpha_{DR})P_t$.

for a simplified layout without need for resistive partition networks and corresponding to operating conditions in the saturation regions (high g_m) for both the FETs.

In order to prevent oscillator load variations due to different RF operating conditions of the mixer as well as to deliver maximum local oscillator RF power with minor mixer conversion losses, a passive splitting network which realizes matching conditions for the oscillator is used in conjunction with a single MESFET buffer stage.

Both for DRO and mixer design, a 300 μm FET was chosen to deliver sufficiently high output power without excessive layout occupation area.

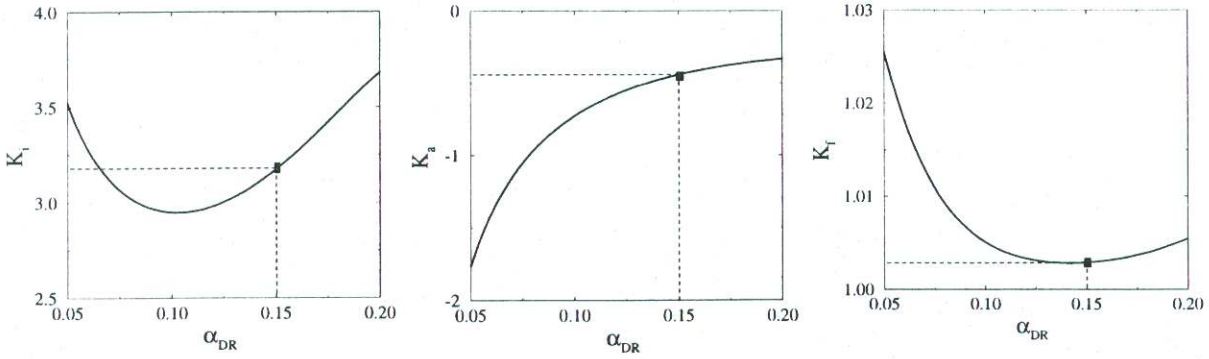

Fig.3: Stability indexes used for oscillator design: k_i instability index, k_a steady-state amplitude stability index, k_f steady-state frequency stability index (see text).

Testing

In Fig.6 a photograph of the circuit (2.2 x 2.7 mm^2), realized through the F20 GEC-Marconi GaAs MMIC process, is presented.

An on wafer characterisation of the final circuit was carried out to evaluate the DC, small-signal and non-linear behaviour of the whole system. The mixer output power is plotted in Fig.7 showing that a minimum conversion loss of only 4dB can be achieved. The measurements were performed (for three different bias conditions) by feeding the mixer RF input port with a -40 dBm power signal at the frequency of 10.02 GHz, and sweeping the LO input power at a frequency of 10 GHz.

In Fig.8 the reflection coefficient of the oscillator at the DR coupling port and the transmission parameter between the same port and the RF input mixer port are plotted. The MESFET device was found, as designed, potentially unstable in the $9.9 \div 10.7GHz$ band. The isolation between the RF input and the oscillator is better than 11 dB.

Finally, the circuit has been bonded on an Allumina substrate and mounted on a shielded test gig with microstrip to SMA transitions. Fig.5 shows the power spectrum of the DRO measured at the RF output port in real operating conditions (DR coupled with the microstrip line). The output power [4] is around 8.5 dBm.

Acknowledgment. The authors wish to thank SIAE Microelettronica (Milano) for the chip bonding on the Allumina substrate.

References

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[2] F.Filicori, G.Vannini, *"A design method for DR-stabilised MESFET oscillators"*, Proc. of GAAS'90, Gallium Arsenide Applications Symposium, Roma, Italy, Apr 1990.

[3] F.Filicori, G.Vannini, *"Frequency stability in resonator-stabilised oscillators"*, IEEE Trans. on Circuits and Systems, Nov 1990.

[4] S.A. Maas *Nonlinear Microwave Circuits*, Artech House, 1988.

[4] The power spectrum shown in the Fig.5 is comprehensive of cable attenuations ($\simeq$ 1dB).

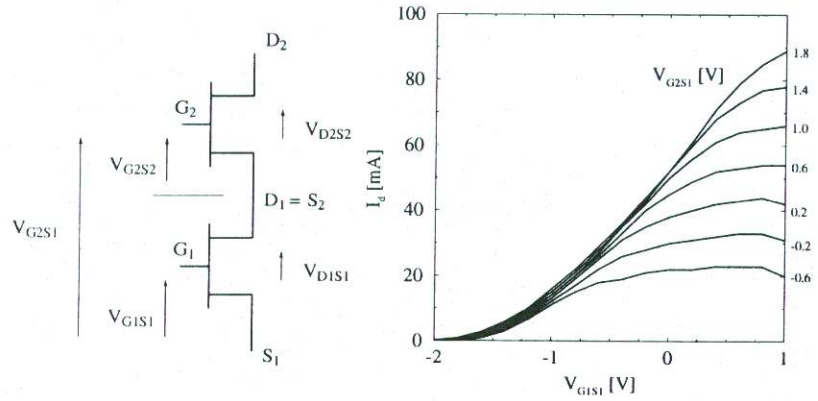


Fig.4: Dual-FET mixer schematic and FET1 Drain current versus applied voltages V_{G1S1}, V_{G2S1}.

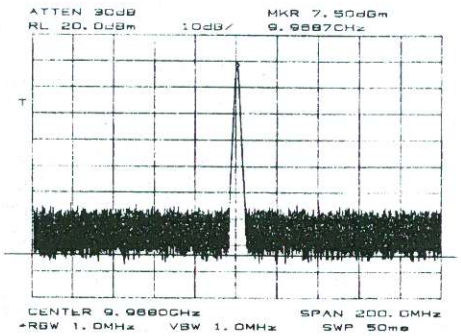


Fig.5: RF output power spectrum.

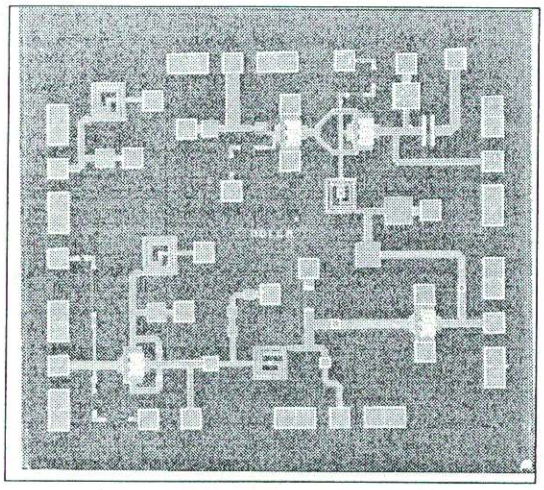


Fig.6: Photograph of the realized circuit (2.2 x 2.7 mm^2).

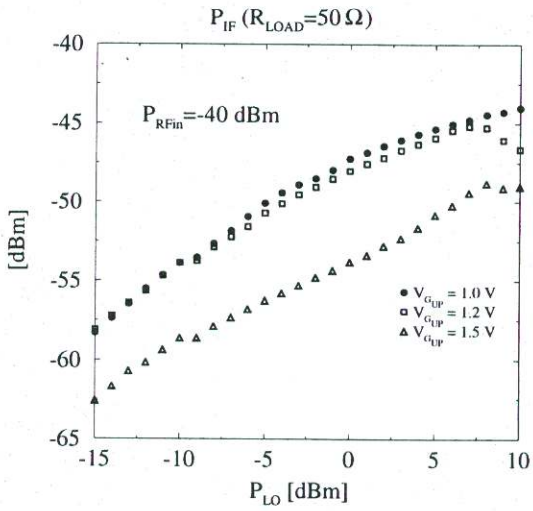
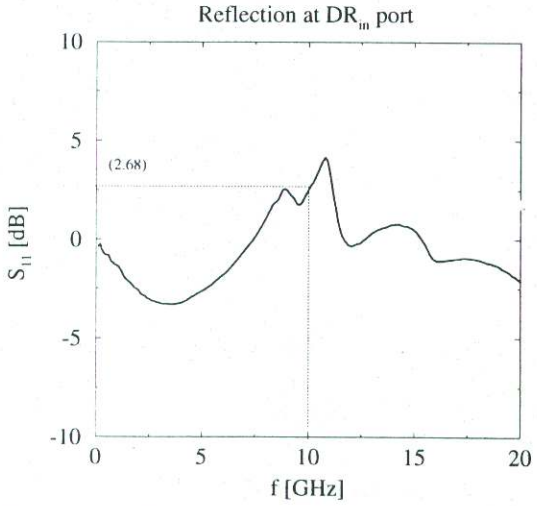


Fig.7: Mixer output power measured as a function of the LO oscillator power.



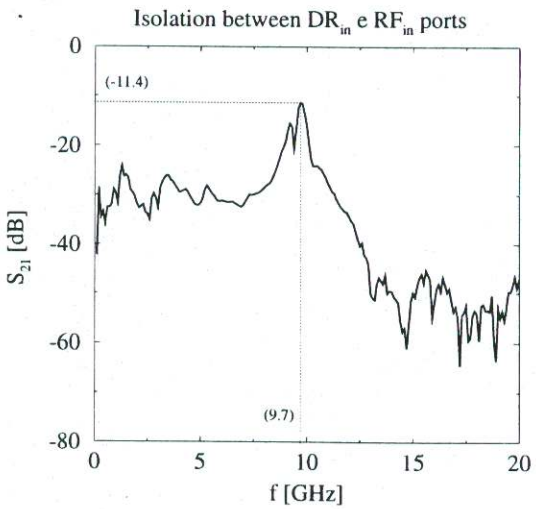


Fig.8: Small-signal on-wafer measurements on the realized circuit. S_{11}: reflection coefficient of the oscillator at the DR coupling port; S_{21}: transmission coefficient between the same port and the RF input mixer port.