A tiny and fully integrated differential VCO for LMDS application

P. Cortese, M.Camiade and D. Domnesque

United Monolithic Semiconductors ,RD 128, BP 46, 91401 Orsay Cedex, France
Tel.: +33 1 69 33 06 27, Fax: +33 1 69 33 05 52, E-Mail : philippe.Cortese@ums-gaas.com

A fully integrated GaAs HBT dual frequency VCO providing a high frequency 18 GHz signal but also a half-frequency 9 GHz signal to a PLL is described. The key advance is achieving good phase noise performance, over a wide frequency band, with very good temperature behaviour and harmonics suppression, at a low cost and small size. More than 3 GHz tuning range is achieved at the 18 GHz port, with 25 dB suppression of fundamental frequency (9 GHz).The 18 GHz VCO yields 5 dBm output power, while on the 9 GHz port it shows more than –10 dBm output power. The chip was assembled in a test jig, then a phase noise of –95 dBc/Hz @ 100 kHz offset was obtained at 9 GHz.

INTRODUCTION

The increasing demand for C-band to K-band communication systems has leaded to a large amount of research and development in the domain of low cost and low phase noise VCO's. Microwave frequency source is commonly recognized as one of the most critical parts of all communication systems used in microwave links. VCO's are very important buildings blocks for radio transceivers, since their performance usually sets the limits on the dynamic range and the jamming sensitivity of a radio transceiver.
The principal requirements for the design of low phase noise oscillators are good quality factor resonator and a low 1/f noise active component. 1/f noise up-conversion has been identified as one of the main contributors to near-to-carrier phase noise and the use of bipolar transistors is therefore preferable to GaAs HEMT. Technologies such as GaAs HBT have demonstrated excellent performances up to Ka band. The next section shows the design of the differential VCO, then in the last section the results and performances will be discussed.

VCO DESCRIPTION

The schematic of the differential core VCO is shown on figure 1.
The topology is a balanced circuit containing two identical and symmetric circuits. Then the two outputs are directly connected to a differential doubler.

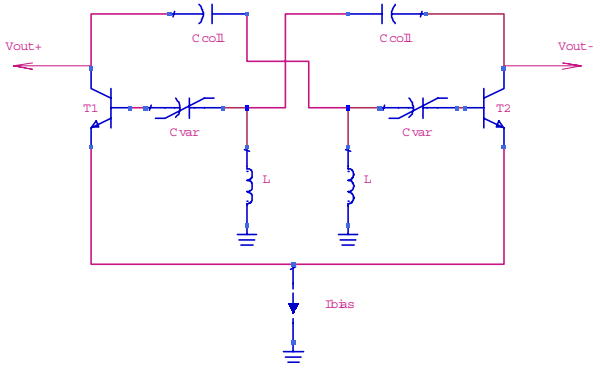


Figure 1: Schematic of the core VCO

The variable capacitance Cvar is implemented by a p+/n- well varactor diode. The tank resonator is composed by the inductor L, the varactor diode capacitor Cvar and the overall capacitor of the circuit.
The transistors T1 and T2 sizes are optimised in order to improve the phase noise performance as well as the temperature behaviour; besides, the circuit assures a sufficient loop gain for oscillation over technology spreads and temperature range (-40°C up to 85°C).
The differential outputs Vout+ and Vout- drive a differential buffer to achieve a stable and sufficient input power over spreads and operating range for the differential doubler. That configuration for the doubler leads to very good fundamental (9 GHz) suppression levels of at

least 25 dBc, due to the topology odd harmonics suppression intrinsic ability. A buffer to achieve low output power variation versus operating conditions and technology spreads follows the doubler. This buffer also includes a filter for unwanted even harmonics.

PERFORMANCES

The results shown on the following plots have been obtained from test jig measurements. The VCO was tested at a supply voltage of 5V and at environment temperature range –40°C to 85°C. On-wafer measurements were also carried out.
The core VCO and the doubler consume 110 mA and 50 mA, respectively. The circuit was designed to operate at 19 GHz with 3 GHz tuning range including extra margin in frequency range (1 GHz) in order to cover the frequency drift due to process and temperature variations. Hence the measured frequency (fig. 2) is in accordance with the simulations.
As the oscillation frequency is determined by the resonator, it is quite insensitive to the other components, especially the transistors. Therefore a slight frequency deviation is observed with the temperature on figure 2, as well as within production spreads.

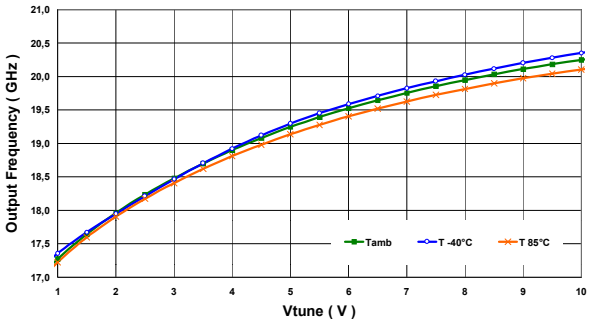


Figure 2 : Measured Output frequency versus tuning voltage

Measurements in figure 3 show an output power at the 18 GHz port greater than 5dBm over the temperature range.

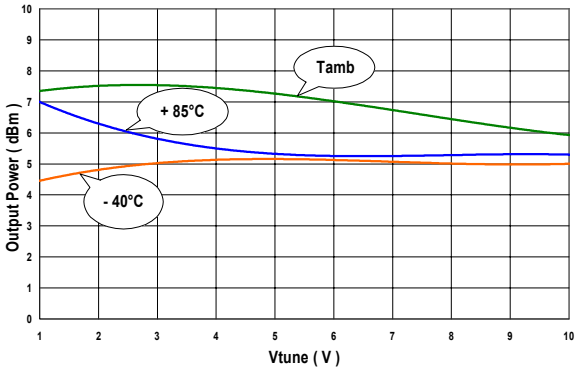
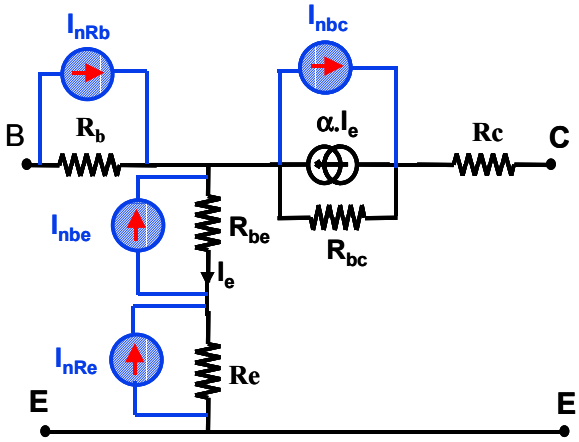


Figure 3 : Output Power @ the 18GHz Port

NOISE CONSIDERATION

In order to predict in the best way the phase noise performances by simulation, the software must be able to simulate such parameters. However it considers the noise levels that they are entered inside the models. Consequently, the low frequency noise model inside the transistors has to be perfectly described. Many measurements were carried out in order to get a model for the transistor used in this design. This model is described below :



Several measurements setups led to reject the I_{nbc} noise source. Therefore the three other noise sources were used in the simulation.
Finally, the phase noise curve shown in figure 4 was measured at 4 V tuning voltage.

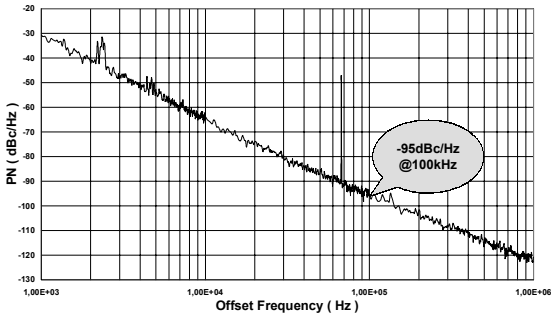


Figure 4 : Measured Phase Noise in dBc/Hz

The very small size for the doubler gives a bare die size of 2.16*1.73 mm².

CONCLUSION

The design and the performances of the dual frequency and differential HBT VCO are described. The circuit provides output signals not only to transceiver circuits at 18 GHz but also to off-chip PLL at 9 GHz. An output power of 5 dBm and a 25 dB suppression of fundamental

frequency (9 GHz) signal at 18 GHz port are achieved. This VCO exhibits a good phase noise of –95 dBc/Hz at 100 kHz offset frequency from the carrier at 9 GHz.
It shall be packaged and surface passivated very soon and the results will be shown in the final paper.

REFERENCES

[1] J.R. BENDER, "Push-Push Design Extends Bipolar Frequency Range", Microwaves & RF October 1983

[2] Y. SUN, T. TIEMAN, H. PFLUG and W. VELTHUIS, " A Fully Integrated Dual-Frequency Push-Push VCO for Wideband Wireless Applications", GaAs-EUMC 2000 Symposium, Paris.