PRECISION WIDEBAND FLIP-CHIP MODELLING

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Abstract - **Techniques are being investigated for development of microstrip flip-chip and rf-through-via MMICs for application over a broad frequency range. In this paper a modelling programme is described which complements such efforts, and provides physical understanding and precise models for the MMIC designer for use beyond X-Band and into the millimetre-wave range.**

I. INTRODUCTION

Flip-chip techniques are widely promoted as the solution for low cost, consistent high performance MMIC bonds at mm-wave frequencies, particularly where automated production is envisaged. A related paper in this conference reviews a broad effort by Marconi Electronic Systems aimed at turning this vision into reality [1]. At low frequencies where the bonds are very short with respect to wavelength they can be treated as simple inductances. However as operating frequencies and bandwidths rise this no longer holds true as other parasitic terms become evident. In principle a large-scale testpiece measurement effort can characterise this quite well. However such an approach does not lend itself to rapid new variations, nor does the s-parameter data it provides leads to an in-depth understanding of the coupling, radiation and resonance effects that can occur. Therefore this paper focuses on how electromagnetic solvers can assist and complement the design process. In our case both classic flip-chip and the alternative rf-through-via configurations are being considered, which adds to the number of possible variables. Use of EM modelling techniques when co-ordinated with practical verification can play a useful and complementary role, particularly if the models can be validated and then subsequently relied upon.

II. MODELLING APPROACH

Although in many respects MMICs and their carrier substrates are planar structures, earlier work and experience had indicated that planar solvers are unsuited for treating such applications. This can be attributed to the inadequate treatment of vertical structures such as vias and plated through holes, and the finite chip substrate area. The MMIC itself , the solder bonds, and the carrier, represent true three dimensional geometric structures complete with complex fields and currents , all of which necessitate the use of a 3D EM solver. If approached in this manner then off-chip fields can be visualised more easily so that, for example, trapped resonances and radiation can be investigated

For models to be representative of measurements the MMICs, and the fully detailed area of the carrier substrates have to be considered. As EM solvers do not easily lend themselves to the analysis of active devices modelling has focused on a series of passive through-line test MMICs. This allows for relatively easy comparison with measurements and subsequent extraction of individual bond characteristics.

III. MODEL DESCRIPTION

In the past, modelling of vias and other structures where there are high current densities has often resulted in somewhat indifferent results. Accuracy is impaired either because the physical shapes are approximated, or due to the basic issue that materials, shapes, and contacts in modelling tools are often more ideal than in practice. These factors are especially important as it is often the wish of the modeller to approximate reality to ease his own task (e.g. for geometry definition), and to avoid excess computer loading and runtimes.

In our work a careful balance has been struck which aims to both minimise compromises, and improve efficiency and confidence in the models. Key to this is that model geometry is defined in considerable detail, including for example blind tapered plated–through holes on the MMIC, and 'passive' solder bumps and pads which are used to provide additional mechanical support for the chip. Such details are visible in Fig.1 and Fig.2 for the Flip-Chip and rf-through-via configurations. In order to both ease the definition task and ensure accuracy, a transfer route has been established using the 2D DXF format so that full MMIC metallisation patterns can be emailed between workers and electronically imported into the 3D models.

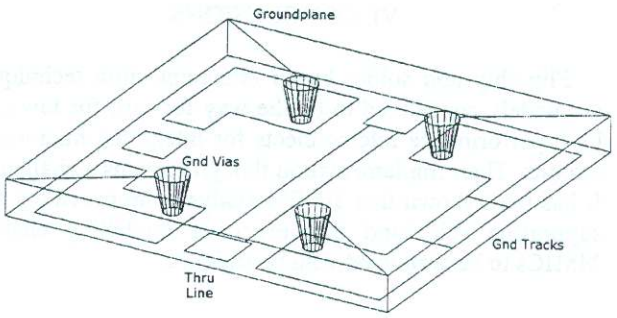

Fig.1 Flip-Chip MMIC Model Geometry

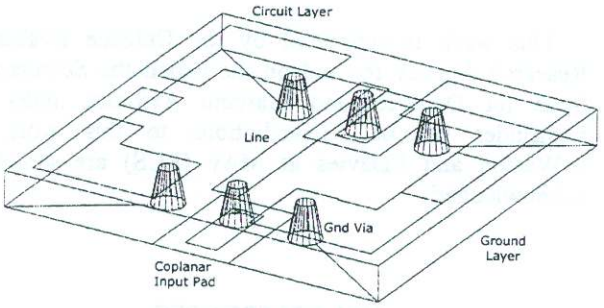

Fig.2 RF-Through-Via MMIC Model Geometry

There they can be combined with the additional details for the solder bonds, plated-through-hole profiles etc. Certain objects such as the bonding pads are defined as distinct entities to make subsequent variations easier to edit.

A further efficiency gain has been obtained by employing a library-based approach. A series of geometry models are separately defined for the MMICs themselves, and the alumina test carriers (which also have solder pads and grounding vias), an example of which is shown in Figure 3. By pre-positioning the geometry in the sub models, assembly of the final analysis models can be readily achieved. This makes certain permutations very flexible, and variations of solder bump profiles easier to incorporate.

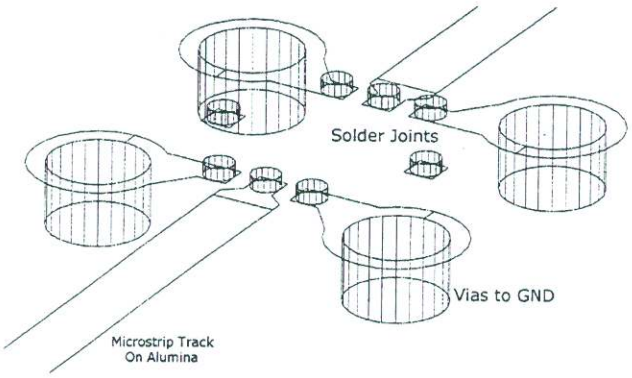

Fig. 3 Alumina Carrier Model with Pre-Positioned Solder Bonds

The precision approach adopted for model geometry, combined with the volume occupied by the carrier, can lead to significant mesh and memory usage. The only explicit measures taken to control these computational burdens, were the use of thin 2D metallisation (i.e. ignoring the small thickness) which minimises mesh aspect ratio problems, and setting the conductor losses to zero. A hidden benefit of our approach is that the majority of the detail is present in areas where the energy densities are highest, which creates a self-seeding effect, helping the mesh to adaptively refine. So although the initial mesh overhead is high, the convergence process is positively assisted. Examples of the overall analysis models are depicted in Fig.4 and Fig.5 for the flip-chip and rf-through-via cases.

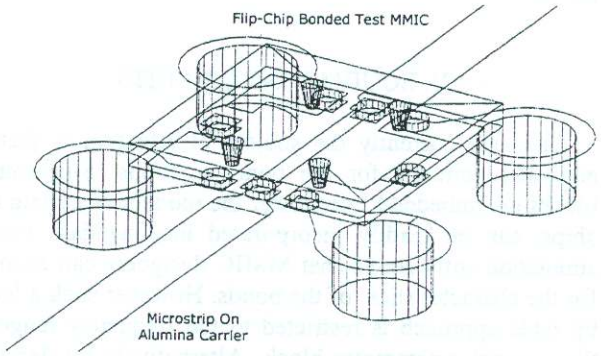

Fig. 4 Flip-Chip MMIC Analysis Model

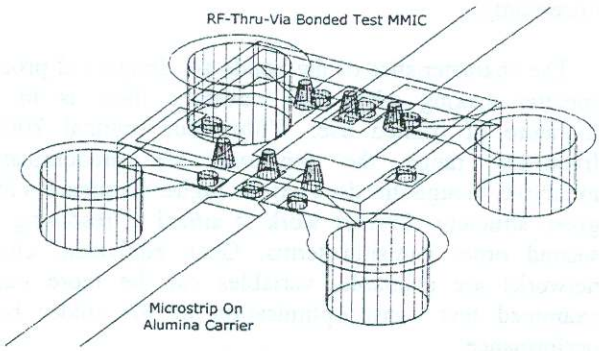

Fig.5 RF-Through-Via Analysis Model

IV. PROGRESS TO DATE

Once the models had been defined initial analysis concentrated on wideband sweeps up to 20GHz. The relatively large carrier substrate volume and geometry detail resulted in 350-400MB of RAM being used, which is well within the capacity of modern workstations. This allowed predictions to be fairly easily compared with test results, without major uncertainties due to measurement calibration/accuracy and radiation/resonance issues. The

frequency range was also more appropriate, as the early MMICs were 100um thick on solder bumps of 120um diameter by 50um high. More recent work in the mm-wave band has been concerned with thinner chips on smaller solder bumps, which give better high frequency performance.

As the operational frequency is raised the potential benefits of the alternative rf-through-via configuration become more apparent. Trapped energy between the chip base and the alumina carrier substrate is reduced and the inductance of the ground plane connections is also lower. The signal layer is now on the upper surface of the MMIC where conventional microstrip design techniques can be applied and the proximity of the carrier substrate is not a factor.

V. EQUIVALENT CIRCUITS

One area currently the subject of attention is that of equivalent circuits for the bond junctions. S-parameter blocks de-embedded from either the models, or certain test chips, can be readily incorporated into standard circuit simulation software so that MMIC designers can account for the characteristics of the bonds. However such a look-up table approach is restricted to the frequency range of the original s-parameter block. Alternatively by deriving the equivalent circuits, frequency interpolation can be more easily applied, and extended beyond the original frequency range of the analysis (though with increasing uncertainty).

The characteristics of the bonds are design and process specific making what little coverage there is in the literature of limited use. Within our original 20GHz frequency range the junctions are predominantly inductive, though this does vary at higher frequencies for a given structure. Current work is aimed at resolving the second order parasitic terms. Once equivalent circuit networks are available, variables can be more easily examined that assist optimisation of the solder bond performance.

VI. CONCLUSIONS

Flip-chip and solder bump interconnection techniques are widely considered to be the way forward for low cost high performance interconnects for integrated microwave circuits. Their implementation though remains a challenge. It has been shown that 3D EM analysis can provide a key supporting role, and that precision modelling enables MMICs to be simulated with confidence.

VII. ACKNOWLEDGEMENTS

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VIII. REFERENCES

[1] I.Davies, W.A.Phillips, G.Humpston, M.J.Niman, "A review of Flip-Chip GaAs Circuits, Models, Interconnections and Modelling Techniques in use at Marconi", GAAS'99