A Model for SiGe MODFETs with Improved Large-Signal Quality and Frequency Range

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Abstract — **A new, analytic large-signal model for N-channel SiGe Modulation Doped Field Effect Transistors (MODFETs) is presented. The model is based on a non-linear equivalent circuit and can be employed to fit the characteristics in the sub-threshold, linear and saturation operating region from DC to high frequencies. In addition to the non-linear I_{ds} current source, gate/drain- and gate/source capacitance elements, it contains a dispersion model to account for the observed low-frequency dispersion effects in the devices.**

This contribution focuses on the reliable prediction of large-signal characteristics such as gain compression and third order intercept points by extending the covered gate-source and drain-source voltage regimes of the model. Device characterisation has been carried out up to 50GHz and allows for the extension of the model's valid frequency range well beyond the device's measured transit frequency of around 40GHz.

I. Introduction

SiGe HEMT (High Electron Mobility Transistor) technology has been proven to attain high speed performance similar to the well-known HEMT based on GaAs, but with the merits of low cost processing and compatibility to other Si-based technologies. In order to make this promising technology available for the design and realisation of high-speed circuits, an efficient non-linear simulation model is required which accurately predicts device behaviour. The described model, developed in conjunction with SiGe HFETs (Hetero-Field Effect Transistor), provides efficient, analytic large-signal expressions needed in circuit design. It does not contain any partially defined expressions which makes it robust with respect to simulations requiring higher order derivatives, e.g. intermodulation evaluations.

II. DC Model

The equivalent circuit including the de-embedding network is shown in Figure 1.

DC characteristics can be well described using the COBRA FET model [1], developed at University College Dublin, which proves to be well suited for modelling of SiGe field effect transistors from the sub-threshold to saturation regions. The transistor used for model development is a $0.13\mu m$ depletion mode SiGe n-channel MODFET fabricated at the DaimlerChrysler Research Center in Ulm, Germany [2] [3]. The device has a threshold voltage of -1.4V and reaches its maximum transconductance of around $170mS/mm$ at $V_{gs} = -0.8V$. Equations 1 - 4 show the COBRA I_{ds} expression, with Greek characters indicating fitting parameters obtained through numerical parameter optimisation.

$$I_{ds}\left(V_{gs},V_{ds}\right) = \beta \cdot V_{eff}^{\left(\frac{\lambda}{num}\right)} \cdot \tanh\left(\alpha V_{ds}\left(1+\zeta V_{eff}\right)\right) \quad (1)$$

where

$$num = 1 + \mu V_{ds}^2 + \xi V_{eff} \quad (2)$$

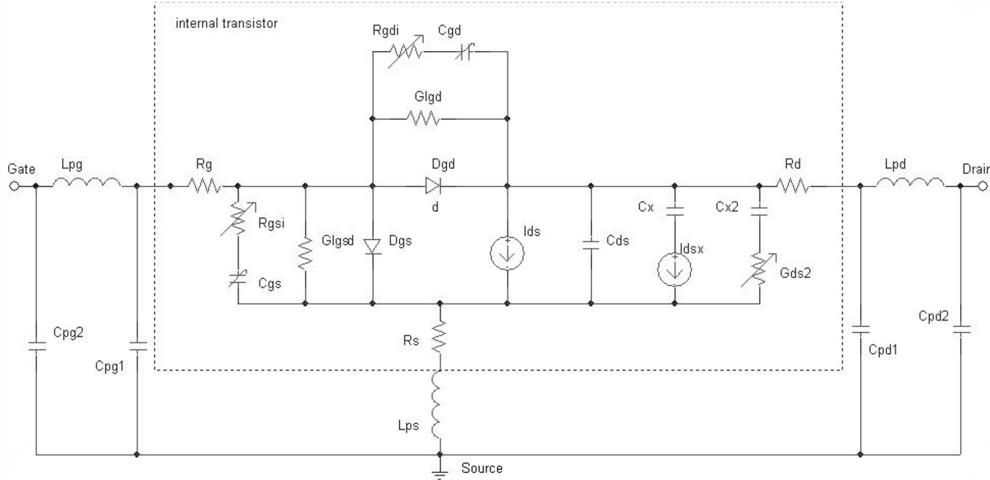

Figure 1: HFET model topology incl. de-embedding network

$$V_{eff} = \frac{1}{2}\left(V_{gs} - V_{t1} + \sqrt{\left(V_{gs} - V_{t1}\right)^2 + \delta^2}\right) \quad (3)$$

$$V_{t1} = \left(1 + \beta^2\right) Vto1 - \gamma V_{ds} \quad (4)$$

DC modelling of previous work usually included gate voltages of -1.5V to 0V and drain voltages from 0V to 1.5V. This covered all transistor operating regions to show the suitability of the COBRA model equations. However, for large-signal simulations with power levels at the device input of above 0dBm, the voltage regime covered by the model has to be extended. In this work, the COBRA I_{ds} expression has been used to model the I_{ds} characteristics in regions of positive gate and high drain voltages. Figure 2 shows the comparison of measured and modelled output characteristics of a $0.13\mu m$ gate length, $108\mu m$ gate width SiGe MODFET using the COBRA function. Drain current output characteristics of the device are obtained through swept measurements. In view of low-frequency (LF) dispersive effects mentioned below, these IV characteristics therefore include any thermal effects due to self-heating of the devices.

III. HF Modelling

A. Model Extraction

After extracting the de-embedding parameters based on a standard circuit topology and using an extraction routine common for HFET structures [4], the non-linear gate capacitance and low-frequency dispersion model is developed. The voltage dependance of the gate-source and gate-drain capacitors is directly modelled through the extracted capacitance data from multi-bias S-parameters, i.e. no gate charge expression is developed. C_{ds} shows relatively weak voltage dependance and is included as a linear element. The current correction source I_{dsx} and conductance G_{ds2} account for the altering of output conductance and transconductance due to frequency dispersive effects observed in the MHz regime and attributed to the presence of charge traps in the HEMT channel region. The resulting large-signal model can be verified in a comparison to DC-, bias-dependent S-parameter as well as large-signal measurements. The modelling and parameter extraction process will be described into more detail in another publication [5]. With the inclusion of LF dispersion, the model becomes accurate from DC up to the GHz regime. New S-parameter measurements for this contribution, carried out in a system setup which allows calibration and device characterisation up to 50GHz, confirm the model's valid

frequency range well beyond the device's transit frequency. Measured transit frequency and maximum frequency of oscillation of the embedded device are found to be 35GHz and 58GHz, respectively. A comparison of measured and simulated S-parameters at a transistor bias point in saturation is shown in Figure 3. The phase error in S_{11} is mainly due to missing non-quasi static resistors R_{gsi} and R_{gdi} in the present large-signal model implementation.

B. Large-signal Verification

Large-signal verification is carried out using gain compression measurements of the fundamental frequency at 2.4GHz as well as power at the 2nd and 3rd harmonic frequencies under various bias conditions taking into account the signal losses in the cable sections surrounding the device under test. Input power at the device input level can be varied from -14dBm to 6dBm. In its first stage of development, the model's large-signal prediction of gain compression and third order intercept points was found to be more restrictive than necessary in comparison to the measured characteristics of the devices. This is caused by the input signal peak voltages at high power levels reaching values close to the Schottky gate built-in voltage, a region where the devices were not characterised and model parameters not extracted. Also, drain-source voltage peaks exceed the valid operating region. For instance, when limiting the parameter extraction process of the non-linear I_{ds} current source to gate-source voltages below the effect of transconductance tail-off, i.e. the area of reduced rate of transconductance roll-off with increasing gate voltages, the model predicts too much gain compression for gate signal peaks reaching high voltage levels. In addition to that, the non-linear dispersion model elements I_{dsx}, G_{ds2} as well as gate capacitance C_{gs} and C_{gd} need to be adapted to larger voltage regimes. Extension of the model validity in regions of positive V_{gs} and high V_{ds} allows improved prediction of large-signal behaviour (Figure 4).

IV. CONCLUSION

A new large-signal model for N-channel SiGe HEMT transistors which includes voltage dependance of gate capacitance and LF dispersion effects has been presented. Analytic, empirical expressions are used to describe the non-linear elements of the equivalent circuit. Enlarging the voltage regime covered by the model equations makes a more reliable large-signal prediction possible. As a result, a model of the SiGe MODFET can now be developed for applications where large-signal behaviour is a critical design aspect.

V. ACKNOWLEDGMENT

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VI. REFERENCES

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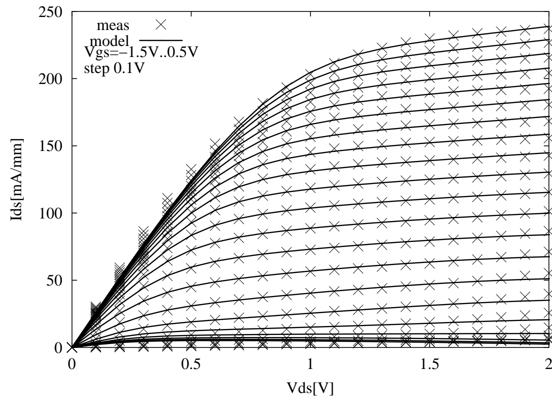

Figure 2: Comparison of measured (swept) and modelled common-source DC characteristics of a $0.13\mu m$ gate length, $108\mu m$ gate width n-channel SiGe MODFET using the COBRA I_{ds} expression.

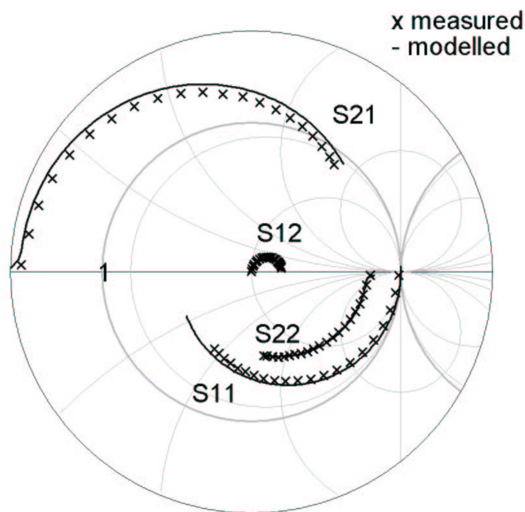

Figure 3: Scattering parameter model verification for frequencies up to 50GHz using the complete large-signal model of a $108\mu m$ gate width transistor in saturation mode. Bias conditions: $V_{gs} = -0.8V$, $V_{ds} = 1.5V$.

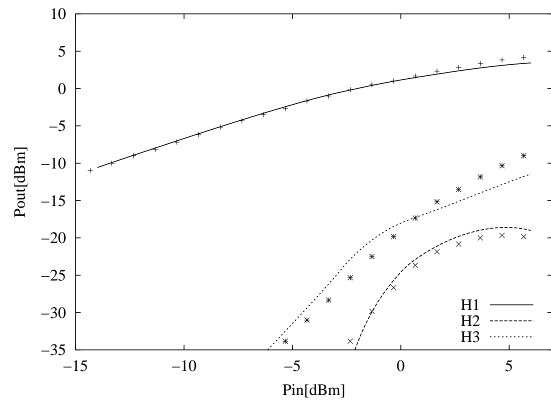

Figure 4: Large-signal model verification using gain compression measurements at 2.4GHz and 2nd and 3rd harmonics. Bias conditions: $V_{gs} = -0.8V$, $V_{ds} = 1.2V$. Lines are simulated, symbols are measured results.