

A broad-band active frequency doubler operating up to 120 GHz

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Abstract — A broad-band monolithic integrated active frequency doubler operating in DC-120 GHz frequency range is presented and compared with several previous versions. The circuit is fabricated in a self-aligned InP DHBT process. Circuit measurements show sinusoidal output waveform at 120 GHz. For -8 dBm input power, the doubler has a maximum conversion gain of -0.25 dB at 50 GHz due to a peaking inductor on the doubler output.

I. INTRODUCTION

Frequency multipliers, and in particular frequency doublers, are important building blocks for many applications, as well as for measurement equipment. The progress of semiconductor technologies based on both specific materials and proper scaling of devices enables to contemplate high speed broad-band system applications up to 100 GHz. Design and measurement of such high speed circuits present important challenges. Specific design methodology should be applied. For measurement, high frequency sources are necessary but usual sources such as manufacturer synthesizers are limited to 60 GHz.

Broad-band active frequency doublers have been described in Si BJT at 12 GHz [1], in SiGe HBT at 42 GHz with 8.6 dB gain [2] and in GaAs pHEMT at 50 GHz with 5 dB loss [3]. Also, others MMIC V-band frequency doublers have been reported (see comparative table in [4]) but these circuits have a limited band of operation. Indeed, their -3 dB output power bandwidth is in the best case around 30 %.

Previous version of the doubler was presented in [5]. In this paper we present the design, fabrication and characterization of a broad-band frequency doubler operating from DC to 120 GHz and comparisons with previous versions. To implement these frequency doublers, we have chosen a Gilbert multiplier structure. This double-balanced architecture allows to achieve good fundamental and odd-harmonics rejection. We have designed four doubler versions. One of them is composed of a Gilbert cell with an input active splitter and an output peaking inductor to achieve multiplication up to 120 GHz. To the author's knowledge, this is the highest frequency of operation for a broad-band active frequency doubler in any technology.

The InP DHBT technology, used for doubler fabrication, is presented in section II, the doubler design

in section III and measurement results up to 120 GHz in section IV.

II. TECHNOLOGY

The InP/InGaAs Double Heterojunction Bipolar Transistor (DHBT) technology developed at Alcatel-Thales III-V laboratory and used for doubler fabrication has been described in detail [6]. It is a complete circuit technology with high performances, particularly suited to fabrication of high speed circuits. Its static and dynamic characteristics are as follows:

- $BV_{CE0} > 7$ V: breakdown voltage measured for a basic current $I_b = 100$ μ A.

- $F_T = 170$ GHz and $F_{MAX} = 210$ GHz: cut-off frequencies at a current density of about 2 mA/ μ m² for 2x10 μ m² emitter transistors (used in doubler).

In Fig. 1 F_T and F_{MAX} frequencies are compared as a function of collector current.

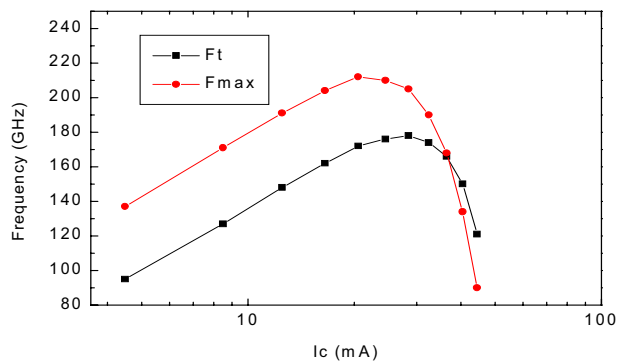


Fig. 1. F_T and F_{MAX} for a 2x10 μ m² emitter transistor

III. CIRCUIT DESIGN

The frequency doubler is based on a Gilbert cell with both inputs connected together as shown in Fig. 2. Frequency multiplication results in generating harmonics due to nonlinear characteristics of the transistors in the Gilbert cell.

A. Electrical design

The first goal of this design was the high frequency of operation (up to 120 GHz). Four integrated doubler versions have been designed with or without various improvements (Table I). The last version is reaching 120 GHz operation.

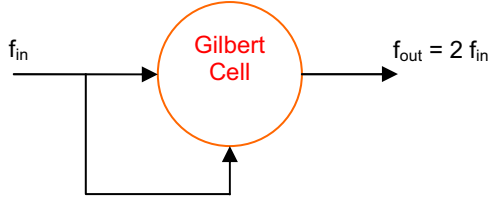


Fig. 2. Gilbert cell as a frequency doubler

The first version (V1), which serves as reference, is the usual Gilbert Cell. This doubler presents only two stages: emitter followers and a Gilbert cell. The circuit is composed of two pairs of emitter followers that feed the LO lower differential pair and one emitter follower pair connected to the RF upper differential pairs (Gilbert cell). These emitter follower stages realize a level shifting and impedance matching. Frequency multiplication occurs in the differential pair stage. Current mirrors act as stable current sources. No output buffer is used: to optimize output swing at high frequencies, the doubler output is directly connected to the Gilbert cell output. In contrast to most Gilbert cells, we have chosen to use only one Gilbert cell output to minimize layout parasitics. Even if the bandwidth power is half the one of a differential output, post-layout simulation demonstrates that for a single-ended application the use of asymmetrical output architecture increases the bandwidth thanks to a strong reduction of output parasitic capacitances.

The second version (V2) adds a peaking inductor on the output in order to improve output amplitude at high frequencies [7]. The peaking inductor (200 pH) has been realized with a Grounded CoPlanar Waveguide line.

V1 and V2 versions use an external frequency splitter to provide the needed two symmetrical inputs. In the third version (V3), we decided to circumvent this problem by using an internal splitter. Only one RF input signal is thus needed plus a reference DC value (REF). Still, the design and layout of V3 version offer the possibility to work in differential mode i.e. with two symmetrical input signals. Doubler block diagram of V3 version is presented in Fig. 3. In this version, the IN input signal is changed by the input active splitter into two symmetrical signals (OUT1 and OUT2). These two signals enter on RF and LO Gilbert cell inputs. They are converted by the cell into an IF output signal of double frequency while the fundamental frequency is suppressed.

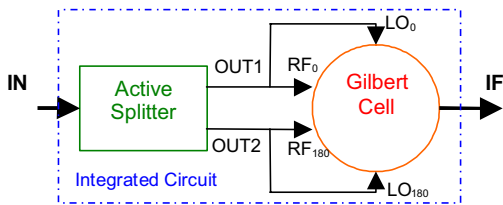


Fig. 3. Block diagram of the frequency doubler

Components \ Versions	Active Splitter	Gilbert Cell	Peaking Inductor
V1		x	
V2		x	x
V3	x	x	
V4	x	x	x

TABLE I
SUMMARY OF DIFFERENT DOUBLER VERSIONS

The fourth version (V4) adds a peaking inductor to V3 version, similarly to V2 version. Fig. 4 shows V4 electrical scheme. The active splitter is composed of a differential amplifier with feedback resistors that provides broad-band amplification. Emitter degeneration is used in the amplifier to linearize output splitter signals.

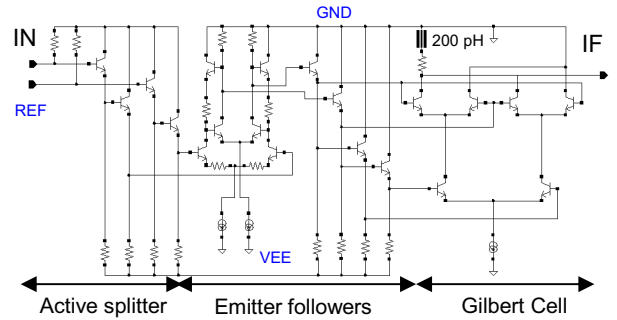


Fig. 4. Electrical scheme of the frequency doubler (V4 version)

B. Layout design

Signal lines (two inputs) are fed via matched 50 Ω GCPW lines. Similarly output signal is connected to output pads with 50 Ω GCPW lines. Signal part of the layout is compacted to shorten high frequency paths. The circuit core is optimized for minimum wire length and maximum symmetry. The chip dimensions are 1400 x 1600 μm^2 . The core footprint is 250 x 350 μm^2 . DC bias connections are decoupled on wafer with RC circuits.

IV. MEASUREMENT RESULTS

The doubler characteristics were measured using on-wafer probing and bias lines. The measurement set-up is composed as follows:

A frequency synthesizer provides a signal up to 60 GHz. Output signal waveform is displayed on an oscilloscope.

65 GHz probes are used at the circuit output. Measurements are realized with remote sampling head (70 GHz) and very short cables. The use of a precision timebase module allows to characterize precisely the time jitter of the doubler.

It is clear from the equipment characteristics, that above 70 GHz our measurements are cumulating hard-to-estimate losses from different measurement elements (probes, cables, sampling head). Indeed, e.g. sampling head data sheet shows the frequency response up to 70 GHz. At 70 GHz head losses are about 2.6 dB but it is very difficult to extrapolate its behaviour above 70 GHz. In the best case, extrapolation is linear but, in the worse case, a bandwidth hole may appear and so losses can be very important. Measurement was realized in spite of these limitations. In consequence, we can estimate the actual bandwidth of the doubler as higher than the measured one.

V1, V2 and V3 doublers were characterized by applying RF signals on input pads (external splitter mode). In addition V3 and V4 were characterized by applying a RF signal on IN pad and a DC reference voltage signal on REF pad (internal splitter mode).

Fig. 5 summarizes measured performance of different doubler versions. Reference output amplitude is 158 mVpp and input power -8 dBm.

We observe an amplitude multiplication by 1.3 between V1 and V2 (as V3* and V4*) due to inductive peaking.

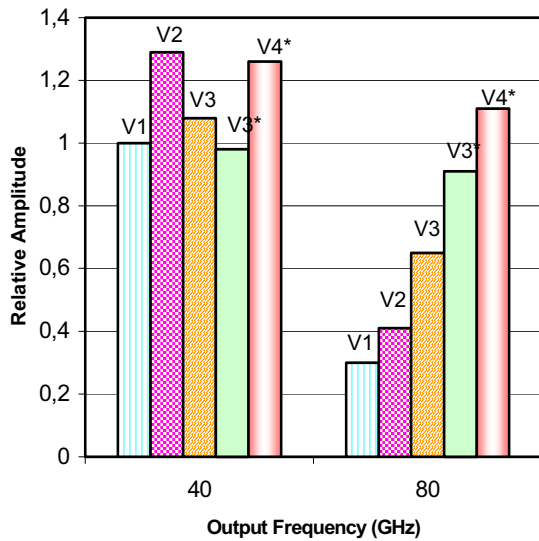


Fig. 5. Doubler performance measurement comparison. V1, V2, V3 differential mode; V3*, V4* reference mode

Let us analyze the effect of active splitter. Two measurement modes of V3 were realized: V3 (external splitter mode - differential operation) and V3* (internal splitter mode - referenced operation). We can note that the ratio between V3 and V3* changes from 40 GHz to 80 GHz. V3* mode of operation is more advantageous for higher frequencies. The explanation of this fact is as follows: when operating with an external splitter (V3*) we need cables and delay lines which have a limited bandwidth. These additional elements induce signal degradation at higher frequencies, making operation with internal splitter more advantageous. However at lower frequencies (40 GHz) differential operation results in better output signal amplitude than the referenced one. At

80 GHz we observe a V4* amplitude increase of 3.7 factor compared to the reference version V1.

V1 and V2 frequency doublers consume 150 mW whereas V3 and V4 frequency doubler consume 730 mW shared between the active splitter (580 mW) and the multiplier (Gilbert cell) core (150 mW). VEE bias voltage is -4.5 V.

Following the reported comparison, more in-depth measurements were carried on the V4 active splitter doubler with internal splitter mode (V4*).

Fig. 6 shows the 60 GHz input signal and the 120 GHz output signal of the V4* frequency doubler. Due to measurement bench losses, the actual output signal amplitude is greater than the measured 9 mVpp.

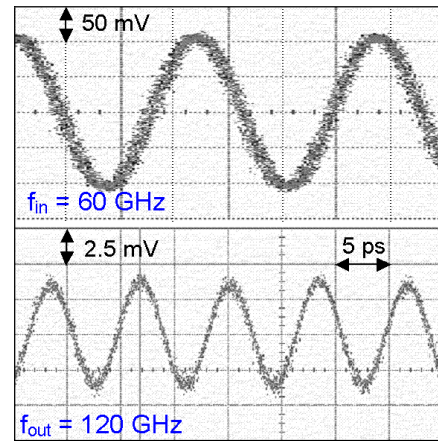


Fig. 6. Measured (top) input and (bottom) output waveforms at 120 GHz (V4*).

In Fig. 7, the V3* and V4* conversion gain versus output frequency is shown for -8 dBm input power. It is necessary to note that above 70 GHz the conversion gain is underestimated because of measurement bench losses. A minimal -3 dB bandwidth from DC to 86 GHz is measured.

We can observe inductive peaking effect. The maximum effect is at 50 GHz when $V4^*/V3^* = 1.4$ (3 dB). So the doubler has a maximum conversion gain of -0.25 dB for -8 dBm input power.

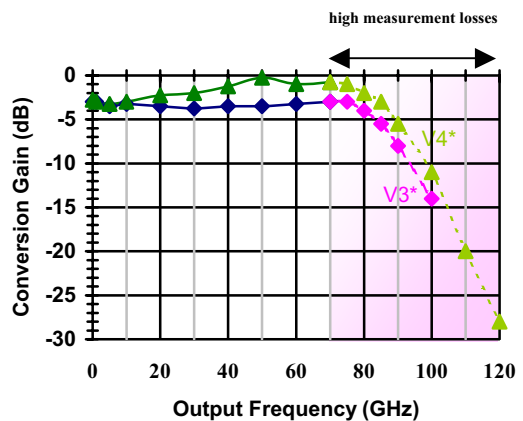


Fig. 7. Measured conversion gain versus output frequency for -8 dBm input power (V3* and V4*).

VI. CONCLUSION

In this paper we presented the design, fabrication and measurements of broad-band frequency doubler operating in state-of-the-art DC-120 GHz frequency range. A Gilbert cell with integrated active splitter architecture and an output peaking inductor allowed to obtain such high frequency. These results were obtained in spite of measurement equipment limitations.

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