EXPERIMENTAL AND NUMERICAL STUDY OF THE HOT ELECTRON DEGRADATION OF POWER AlGaAs/GaAs HFETs

G. Sozzi, D. Dieci°, R. Menozzi, C. Lanzieri*, T. Tomasi° and C. Canali°

Dipartimento di Ingegneria dell'Informazione, University of Parma
Parco Area delle Scienze 181A, 43100 Parma, Italy
Tel. +39-0521-905811 / Fax +39-0521-905822 / e-mail g_sozzi@ee.unipr.it

° Dipartimento di Scienze dell'Ingegneria and INFM, University of Modena and Reggio Emilia
Via Campi 213/B, 41100 Modena, Italy

* Alenia Marconi Systems, Via Tiburtina km 12.400, 00131 Roma, Italy

ABSTRACT

This work investigates, through the use of numerical drift-diffusion simulations, the hot electron degradation mechanisms of power AlGaAs/GaAs HFETs. The experimentally observed degradation modes can be consistently explained by a negative charge storage at the device surface over the gate-drain access region.

INTRODUCTION

AlGaAs/GaAs HFETs are promising devices for power amplification at X- and Ku-band (1)-(4). Their combination of a relatively low-doped AlGaAs barrier layer and n-doped GaAs channel offers performance advantages over traditional GaAs MESFETs at a much lower cost than that of AlGaAs/InGaAs PHEMTs. Since a very large potential HFET market exists in wireless telecommunication applications, many studies have been recently carried out and published on different aspects of HFET design, fabrication and performance.

In particular, reliability is a key issue for extensive industrial exploitation. While material and contact-related issues have been abundantly dealt with in the last two decades for the AlGaAs/GaAs system, only recently the assessment of hot electron reliability hazards has surfaced in the open literature (5). High-field effects are indeed a key issue for power FETs, and some papers have recently addressed the design and fabrication of high-breakdown-voltage devices (6), (7). As an extension of our previous work on hot electron stressing and degradation of power AlGaAs/GaAs HFETs, this work investigates the physical mechanisms that underlie the stress-induced changes of the device electrical characteristics. For the first time, we use two-dimensional, drift-diffusion numerical simulations to support our interpretation of the experimental results.

SAMPLES AND EXPERIMENTS

A. Samples

The HFETs (see Fig. 1 for the cross-section) were fabricated with a double-recess process in production at Alenia Marconi Systems. The bottom-up structure is as follows: GaAs SI substrate; AlGaAs/GaAs multi-layer buffer; 75 nm n-GaAs channel (4 10^{17} cm^{-3}); n-$Al_{0.25}Ga_{0.75}As$ barrier (2 10^{17} cm^{-3}), 30 nm thick in the deep recess region under the gate; n^+-GaAs ohmic cap.

The gate metal is a 0.2 µm Ti layer with a 0.45 µm Al cap on top of it. 1 µm long Ti/Al gates are deposited after wet etching the deep recess; then the gate length is reduced (to 0.7 µm for the HFETs of this work) by selective lateral dry etching of the Ti. The gate width is 4x50 µm. The deep recess is 1 µm wide, and the total drain-source spacing is 5 µm. 300 nm of plasma-deposited SiN passivate the surface.

Typical HFETs feature I_{DSS} = 300 mA/mm and g_m = 150 mS/mm, while V_T varies from –2.5 to –3 V. The two-terminal drain gate breakdown voltage (BV_{DG}^{OFF}), defined at I_G = -1 mA/mm, ranges from 14.2 to 16.4

V. At 10 GHz and 1-dB compression, the HFETs deliver 0.5 W/mm output power, with a gain in the range of 8.5 dB.

B. Stress Experiments

The hot electron stress was performed at room temperature under DC bias. In order to apply accelerated, off-state hot electron conditions to the HFETs under test, the source electrode was kept floating, while the drain-gate diode was driven with a reverse gate current that increased at each stress step. Each step had a duration of 25 hours. After 725 hours, at the end of the stress, I_G = -3.3 mA/mm (a value significantly larger than the widely-accepted safety limit of –1 mA/mm) and V_{DG} = 21.9 V.

EXPERIMENTAL STRESS RESULTS

Fig. 2 shows the HFET output characteristics before and after 725 hours of hot electron stress. A remarkable degradation of I_{DSS} appears after stressing. Both the linear and saturated transconductance are degraded by the stress, as illustrated by Fig. 3.

The I_{DSS} and g_m reductions are connected with a 53% increase of the drain resistance (R_D), as measured using an *end resistance* technique (the source parasitic resistance is practically unmodified by the stress).

On the other hand, the off-state two-terminal breakdown voltage, BV_{DG}^{OFF}, improves significantly (by 51%) after the stress. The on-state breakdown gets better, too: the impact-ionization-generated gate reverse current is remarkably reduced after the stress.

This set of degradation modes, namely $\Delta I_{DSS} < 0$, $\Delta g_m < 0$ (also known as *power slump* (8), (9)), $\Delta R_D > 0$, and the breakdown voltage increase (*breakdown walkout* (10)-(12)), has been often explained assuming surface state creation and electron trapping at the interface between the semiconductor and the SiN passivation over the gate-drain access region. The negative charge storage makes the surface potential more negative; consequently, surface depletion is enhanced, which makes R_D increase and degrades I_{DSS} and g_m. On the other hand, this increased surface depletion is believed to reduce the peak longitudinal electric field in the device channel, hence the improvement of the breakdown voltage.

NUMERICAL SIMULATIONS

In order to validate the surface charge theory of the HFET degradation, we performed two-dimensional, drift-diffusion numerical simulations using a commercial software tool.

The simulated HFET cross-section is shown in Fig. 4. While the layer thickness and doping values replicate the nominal HFET figures as accurately as possible, two simplifications have been introduced in our simulations: (i) a single-recess, vertical-walls gate region has been simulated for simplicity; (ii) since the simulator we use cannot deal with quantum effects such as tunneling, the actual surface alloyed ohmic contacts cannot be implemented; consequently, we placed the source and drain contacts vertically on the device sides.

The low-field electron mobility and the saturated velocity values we used for the GaAs channel are 3263 $cm^2/(V\ s)$ and 1.5 10^7 cm/s, respectively. For the sake of numerical convergence, the drift velocity vs. electric field curve does not show the velocity overshoot and the negative differential mobility region; a monotonic, Silicon-like model was used instead.

A negative fixed surface charge density of 2 10^{12} cm^{-2} was placed over both the source-gate and drain-gate access regions in order to get a reasonable match between the measured and simulated HFET characteristics. Since our main purpose was the comparison of the pre-stress and post-stress simulations, we did not go through a systematic adjustment of the simulation parameters aimed at the best achievable match with the measurements.

For the simulation of the post-stress characteristics, the negative fixed surface charge density was increased to 4 10^{12} cm^{-2} between gate and drain, in order to validate the surface charge theory of the hot electron HFET degradation.

The pre-stress and post-stress simulated I_D-V_{DS} output curves are shown in Fig. 5. The I_{DSS} degradation caused by the increased negative surface charge over the gate-drain region resembles that of Fig. 2 reasonably well.

The linear and saturated g_m compressions are also accounted for by our simulations, as depicted in Fig. 6 (although the quantitative agreement with the measured data is rather poor for the linear case).

As far as breakdown walkout is concerned, the drift diffusion model obviously does not account for carrier heating, therefore no direct investigation of the effect of the gate-drain surface charge on the breakdown voltage can be simulated. Nevertheless, the observation of the simulated channel electric field profiles allows to gain sufficient insight of this phenomenon. Fig. 7 shows the distribution of the longitudinal (i.e., parallel to the current flow) field along the HFET channel (although the transverse field component is quite large, it does not contribute to channel electron heating), both before and after the simulated stress. The bias point is V_{DS} = 6 V and V_{GS} = -2 V; the V_{GS} value corresponds to the maximum impact ionization condition experimentally observed in the actual HFETs, relevant for on-state breakdown. The electric field profile is broadened in the post-stress simulation, and its peak value reduced. This demonstrates that the same negative surface charge storage between gate and drain that prompts the I_{DSS} and g_m degradation is responsible for the beneficial breakdown walkout.

However, it should be pointed out that that the stress-induced surface charge does not cause such electric field lowering under all bias conditions. Fig. 8 depicts the V_{GS} dependence of the peak electric field in the middle of the channel (at V_{DS} = 6 V) for both the pre-stress and post-stress HFET simulations.

It emerges from Fig. 8 that the peak field in the stressed HFET is basically fixed by the surface charge distribution between gate and drain, which makes it practically independent of V_{GS}. It turns out therefore that the beneficial effect of the negative surface charge exists only at low V_{GS}. However, since such low-V_{GS} conditions are typically the most critical for electron heating and impact ionization (the peak field is roughly proportional to $V_{DG} = V_{DS} - V_{GS}$; in our HFETs, the impact-ionization-generated reverse I_G peaks at about V_{GS} = -2.2 V), the simulations indicate that an improvement of the breakdown voltage can be expected after stressing, as indeed was found in our experimental hot electron degradation assessment.

CONCLUSIONS

In this work we investigated the physical mechanism underlying the degradation of hot-electron-stressed power AlGaAs/GaAs HFETs. The devices undergo I_{DSS} and g_m reduction after stressing, as well as breakdown walkout.

Two-dimensional, drift-diffusion numerical simulations show that the measured degradation can be consistently explained by electron capture at the semiconductor-SiN interface over the drain-gate access region. This negative charge accumulation lowers the surface potential, thus widening the depleted region and increasing the drain resistance. A beneficial by-product of this phenomenon is the reduction of the peak longitudinal electric field in the channel, which yields breakdown walkout.

ACKNOWLEDGEMENTS

This work was partly supported by the italian Consiglio Nazionale delle Ricerche through the MADESS II project, and by NATO. The authors are grateful to Mr M. Messori (University of Modena and Reggio Emilia) for technical assistance.

REFERENCES

(1) P. Saunier, W. S. Kopp, H. Q. Tserng, Y. C. Kao and D. D. Heston, "A heterostructure FET with 75.8-percent power added efficiency at 10 GHz," 1992, *IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 635-638.

(2) D. T. Bryant, K. Salzman and R. Hudgens, "Ku-band monolithic 7-Watt power amplifier using AlGaAs/GaAs 0.25-μm T-gate heterostructure FET technology," 1993, *IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 1373-1376.

(3) S. Goto, K. Fujii, H. Morishige, S, Suzuki and S. Sakamoto, "A 100W S-band AlGaAs/GaAs heter-structure FET for base stations of wireless personal communications," 1998, *IEEE Proc. GaAs IC Symp.*, pp. 77-80.

(4) I. Takenaka, H. Takahashi, K. Asano, K. Ishikura, J. Morikawa, K. Sato, I. Takano, K. Hasegawa, K. Tokunaga, F. Emori and M. Kuzuhara, "L/S-band 140W push-pull power AlGaAs/GaAs HFETs for digital cellular base stations," 1998, *IEEE Proc. GaAs IC Symp.*, pp. 81-84.

(5) D. Dieci, R. Menozzi, C. Lanzieri, L. Polenta and C. Canali, "Hot electron effects on $Al_{0.25}Ga_{0.75}As/GaAs$ power HFET's under off-state and on-state electrical stress conditions," to be published on *IEEE Trans. Electron Devices.*

(6) K. Asano, Y. Miyoshi, K. Ishikura, Y. Nashimoto, M. Kuzuhara and M. Mizuta, "Novel high power AlGaAs/GaAs HFET with a field-modulating plate operated at 35V drain voltage," 1998, *IEDM Tech. Dig.*, pp. 59-62.
(7) N. Hara, Y. Nakasha, T. Kikkawa, H. Takahashi, K. Joshin, Y. Watanabe, H. Tanaka and M. Takikawa, "Low-distorsion GaAs-based field effect transistors with InGaP channel layer for high-voltage operation," 1998, *IEDM Tech. Dig.*, pp. 63-66.
(8) H. Hasegawa, K. Katsukawa, T. Itoh, T. Noguchi and Y. Kaneko, "High reliability power GaAs MESFET under RF overdrive condition," 1993, *IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 289-292.
(9) Y. A. Tkachenko, Y. Lan, D. S. Whitefield, C. J. Wei, J. C. M. Hwang, L. Aucoin and S. Shanfield, "Gradual degradation under RF overdrive of power GaAs field-effect transistors," 1993, *Proc. GaAs Reliability Workshop*.
(10) P. C. Chao, M. Shur, M. Y. Kao and B. R. Lee, "Breakdown walkout in AlGaAs/GaAs HEMT's," 1993, *IEEE Trans. Electron Devices*, vol. 39, pp. 738-740.
(11) R. Menozzi, P. Cova, C. Canali and F. Fantini, "Breakdown walkout in pseudomorphic HEMTs," 1996, *IEEE Trans. Electron Devices*, vol. 43, pp. 543-546.
(12) Y. C. Chou, G. P. Li, Y. C. Chen, Y. C. Chen, C. S. Wu, K. K. Yu and T. A. Midford, "Off-state breakdown effects on gate leakage current in power pseudomorphic AlGaAs/InGaAs HEMT's," 1996, *IEEE Electron Device Lett.*, vol. 17, pp. 479-481.

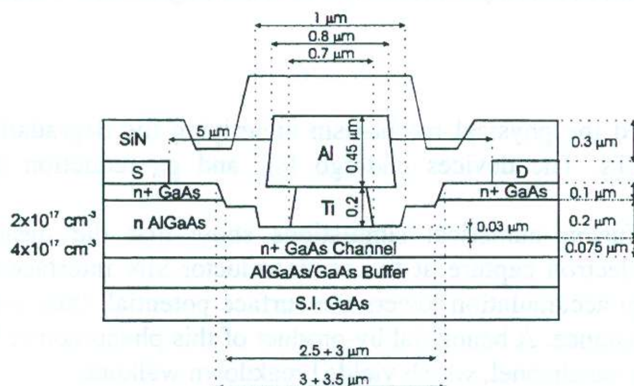

Fig. 1 – Schematic cross-section of the HFETs under test.

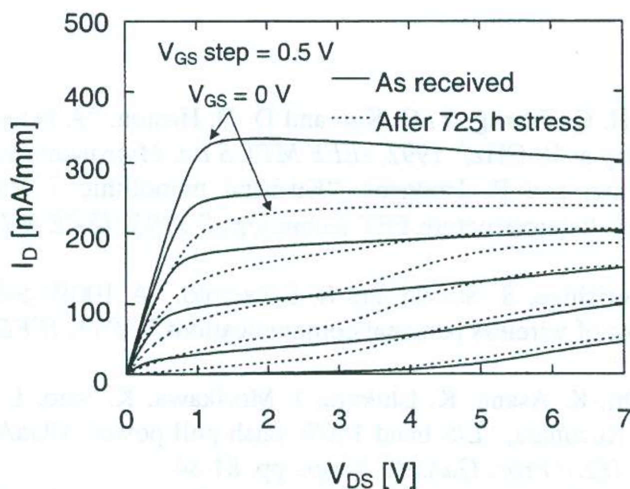

Fig. 2 – Output characteristics of one of the HFETs under test, before and after the hot electron stress.

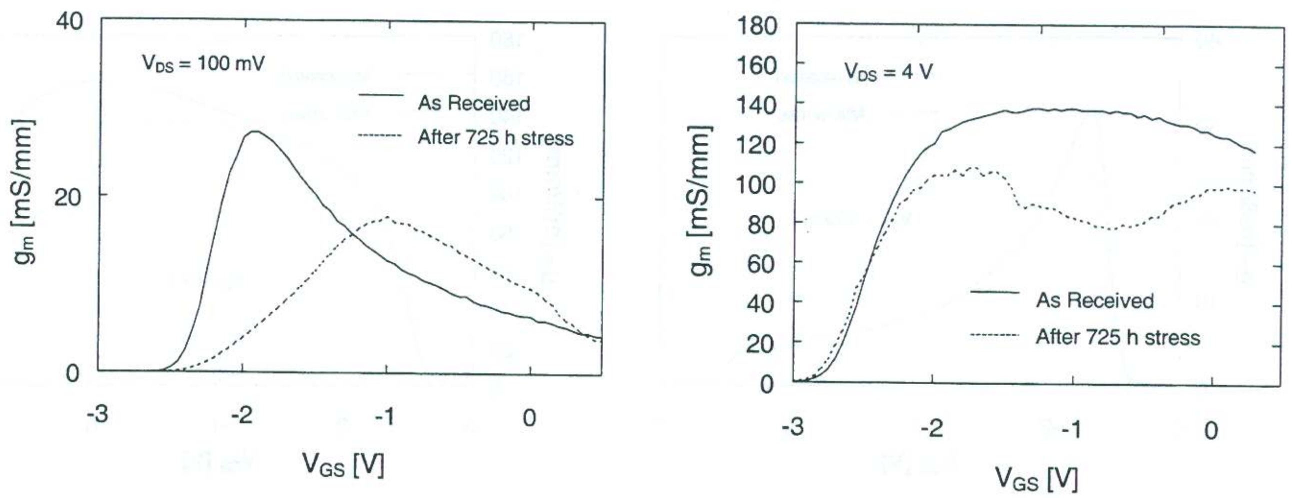

Fig. 3 – HFET transconductance as a function of the gate-source bias, measured in the linear region (left) and in saturation (right) before and after the hot electron stress.

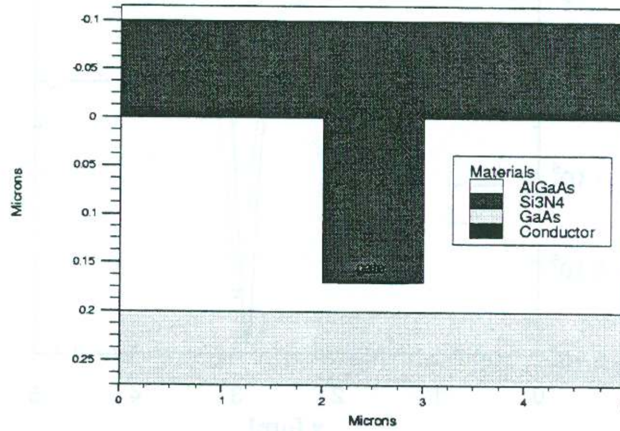

Fig. 4 – Simulated HFET cross-section.

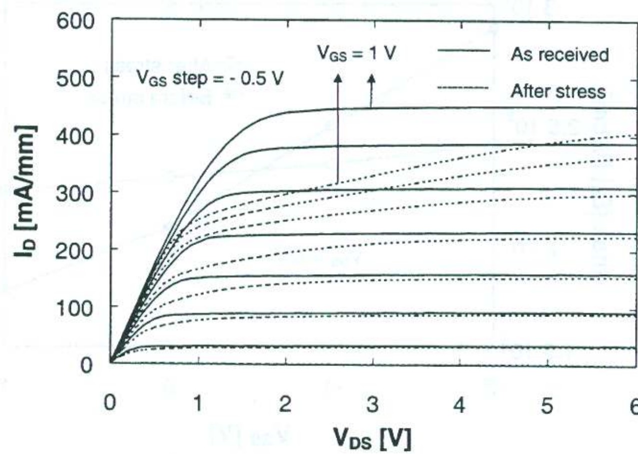

Fig. 5 – Simulated HFET output characteristics, before and after the hot electron stress.

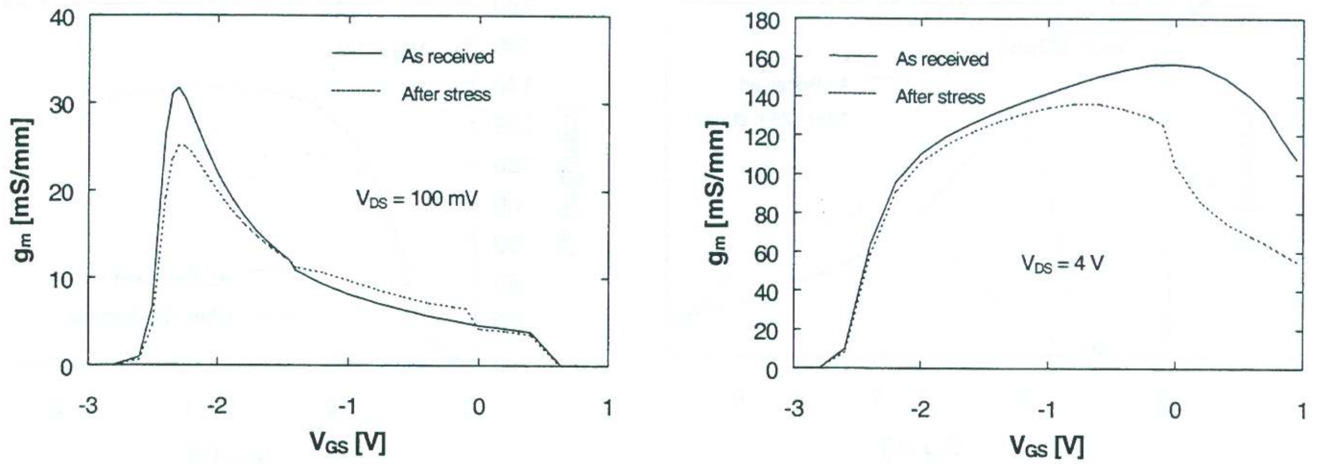

Fig. 6 – Simulated HFET transconductance as a function of the gate-source bias in the liner region (left) and in saturation (right) before and after the hot electron stress.

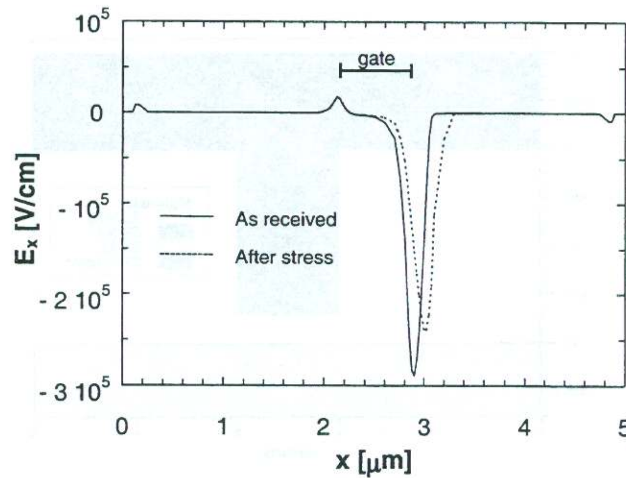

Fig. 7 – Simulated longitudinal electric field along the HFET channel at V_{DS} = 6 V, V_{GS} = -2 V, before and after the hot electron stress.

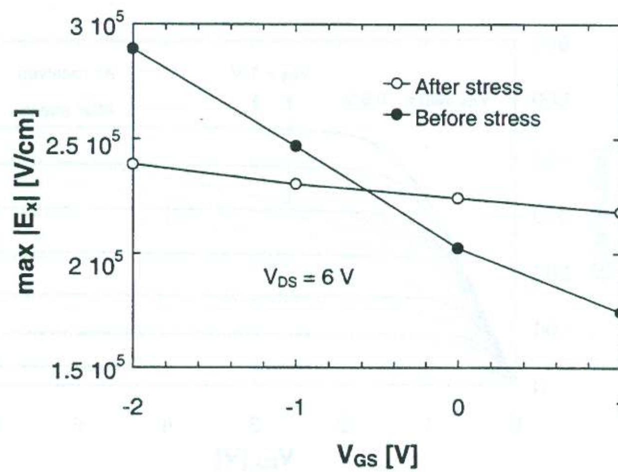

Fig. 8 – Simulated gate-source voltage dependence of the peak channel longitudinal electric field before and after the hot electron stress.