The processing and scalability of AlGaN/GaN HEMTs

B. Jacobs[1], F. Karouta[1], J.J.M. Kwaspen[1], P.R. Hageman[2], L.M.F. Kaufmann[1], P.K. Larsen[2]

COBRA Inter-University Institute on Communication Technology
Eindhoven University of Technology – Department of Electrical Engineering
P.O. Box 513, NL-5600 MB Eindhoven, The Netherlands
Phone: +31 40 247 5116, Fax: +31 244 8375, e-mail: B.Jacobs@tue.nl

Experimental Solid State Physics III, RIM, University of Nijmegen,
P.O. Box 9010, NL-6500 GL Nijmegen, The Netherlands

I. ABSTRACT

This paper presents a discussion on the processing of AlGaN/GaN HEMTs with different gate widths but all with an optically defined 1 µm gate length. Scalability of transistor parameters will be discussed and a small-signal equivalent circuit is extracted which shows the influence of the processing of the Schottky and ohmic contacts.

II. INTRODUCTION

HEMTs based on the AlGaN/GaN material system are expected to be excellent candidates for high power high frequency electronics. High breakdown fields allow high drain-source voltages while the saturation velocity for electrons enhances high frequency operation. However, for high power applications there are some problems related to the heat dissipation. An important improvement is seen when using SiC as a substrate instead of sapphire, Gaska et al [1]. High power densities have been achieved at X-band frequencies. However scaling the transistors towards larger gate widths showed deterioration in performance, Nguyen et al [2].
In this paper the processing and characteristics of AlGaN/GaN HEMTs with gate widths ranging from 10 to 200 µm will be discussed.

III. GROWTH AND PROCESSING

The HEMT structure used in this work was grown at the University of Nijmegen. It consisted of a 30nm GaN nucleation layer on a sapphire substrate. This was followed by a 1 µm thick un-intentionally doped GaN layer, 50nm Si-doped GaN, a 3nm un-intentionally doped $Al_{0.2}Ga_{0.8}N$ spacer layer and a 30nm Si-doped $Al_{0.2}Ga_{0.8}N$ donor layer. This structure was already used by Sullivan et al [3].
For device isolation mesas were etched using conventional Reactive Ion Etching (RIE), Karouta et al [4]. The wafer was first covered with 300nm SiN_x (PECVD). The nitride mask was patterned using S1805 photoresist. To open the nitride mask we used a dry etch (RIE) with a SF_6:Ar gas mixture (10:10 sccm, 40 mTorr at 105W) for 3 minutes. The etch rate for the SiN_x mask was estimated at 220 nm/min. After the dry etch the remaining resist was removed using

acetone and ipa, however resist residues could be seen near the mesas. These residues resulted from reactions between the plasma and resist. To remove these, an oxygen plasma was used (RIE 50 sccm O_2, 200 mTorr at 105W for 1 min.). Currently, the oxygen plasma is used directly after the SF_6:Ar etch. This way, no resist residues are present near the mesas.

The AlGaN donor layer was etched (RIE) using a $SiCl_4$:Ar gas mixture (10:10 sccm, 40 mTorr at 105W for 4 minutes). This resulted in a mesa height of 60nm. Currently, work is being done to achieve sloped sidewalls to etch higher mesas. The remaining SiN_x was etched using buffered HF. Again, some residues could be seen near the mesas which presumably are some SiN_xCl_y compounds. These compounds could easily be removed using acetone and ipa.

For ohmic contacts a Ti/Al (35/115nm) metallization scheme was used. The contacts were annealed for 30 sec. in an Ar ambient at 600^0C. For the gate Ni/Au (20/200nm) was used. All the gates were optically defined with a gate length of 1μm. Gate widths varied between 10 and 200μm.

IV. ELECTRICAL CHARACTERIZATION

DC characteristics were measured using a HP4141. Figures 1(a) and 1(b) show the drain-source current of a 160μm wide transistor as a function of the gate-source and drain-source voltage respectively. In Figure 1(b) the self-heating effect is clearly visible.

RF measurements on this transistor using a HP8510b yielded a F_t of 10.9 GHz and a F_{max} of 19.3 GHz.

The maximum drain-source current, the DC transconductance, F_t and F_{max} are illustrated as a function of gate width in Figures 2(a), 2(b) and 2(c) respectively. Both the transconductance and maximum drain-source current density are decreasing with gate width most likely due to the self-heating effect. Furthermore, F_t depends on the gate width. Using the ideal expression $F_t=g_m/2\pi C_{gs}$, F_t should not scale with gate width as both the gate-source capacitance and the transconductance are proportional to the gate width. However, this expression is only valid when there is no feedback (i.e. the gate-drain capacitance is zero). To verify this condition the maximum stable gain ($MSG=|S_{21}/S_{12}|$) is plotted as function of frequency (Figure 3). It can be clearly seen that for small transistors the MSG is very low and for frequencies above 1 GHz the transistor behaves mostly like a passive network. Hence, the aforementioned equation should not be used for small transistors with very low transconductances.

A small-signal equivalent circuit (Figure 4) was extracted for each transistor. Compared to most other HEMT models there are two additions: a resistor parallel to the gate-source capacitance and a resistor parallel to the gate-drain capacitance. These resistors represent the leakage of the Schottky diode (=112 μA DC for a 200μm wide transistor at 10 V). Furthermore, the extrinsic drain and source resistances are very high which is most likely related to the contact resistance. The contacts were annealed at 600^0C which has been shown to give high contact resistances, Liu and Lau [5]. Either the annealing temperature has to be increased or another metallization scheme (Ti/Al/Ni/Au) has to be used.

CONCLUSIONS

AlGaN/GaN HEMTs with gate lengths of 1um and gate widths up to 200μm were demonstrated. Maximum current densities were measured up to 560mA/mm for 10 μm wide transistors. The 200 μm wide transistor gave an Ft of 10.9 GHz and a Fmax of 19.3 GHz. It was shown that the self-heating effect which increases with gate width degrades the DC performance of the transistors. F_t scaled with gate width which is due to the fact that the behavior of small transistors was mostly passive. The Ti/Al metallization scheme and Schottky contact needs to be improved.

ACKNOWLEDGEMENTS

The authors would like to acknowledge the support of the Dutch organization for applied scientific research (TNO-FEL).

REFERENCES

[1] R. Gaska, A. Osinsky, J.W. Yang and M.S. Shur
Self-Heating in High Power AlGaN-GaN HFET's
IEEE-EDL, Vol.19, No.3, March 1998, pp. 89-91

[2] N.X. Nguyen, C. Nguyen and D.E. Grider
Device Characteristics of scaled GaN/AlGaN MODFETs
Electronics Letters, Vol.34, No.8, April 1988, pp. 811-812

[3] G.J. Sullivan, M.Y. Chen, J.A. Higgins, J.W. Yang, Q. Chen, R.L. Pierson and B.T. McDermott
High-Power 10-GHz Operation of AlGaN HFET's on Insulating SiC
IEEE-Electron Device Letters, Vol.19, No.6, June 1998, pp. 198-199

[4] F. Karouta, B. Jacobs, P. Vreugdewater, N.G.H. v. Melick, O. Schoen, H. Protmann, M. Heuken
High Etch Rate and Smooth Morphology Using a Novel Chemistry in Reactive Ion Etching of GaN
Electrochemical and Solid State Letters, 2 (5), May 1999, pp. 240-241.

[5] Q.Z. Liu and S.S. Lau
A Review of the Metal-GaN Contact Technology
Solid-State Electronics, Vol.42, No.5, 1998, pp. 677-691

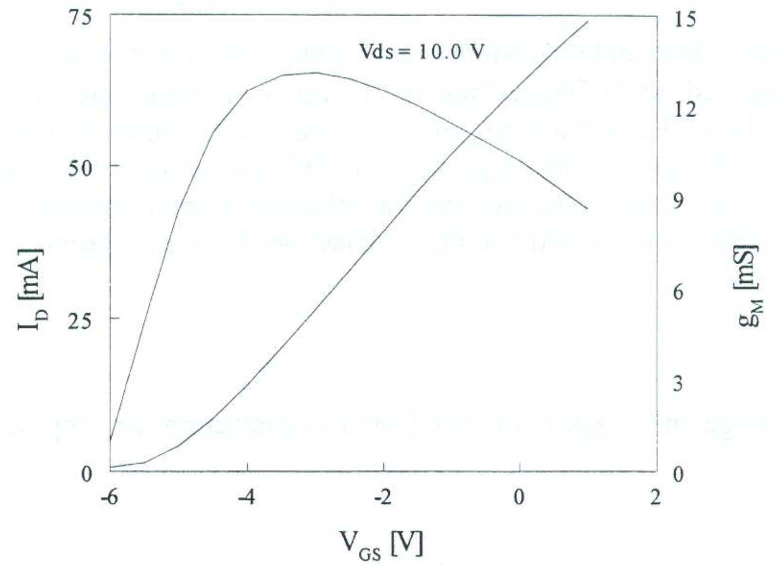

Figure 1a:
The drain-source current and transconductance for a 160μm wide transistor as function of gate-source voltage

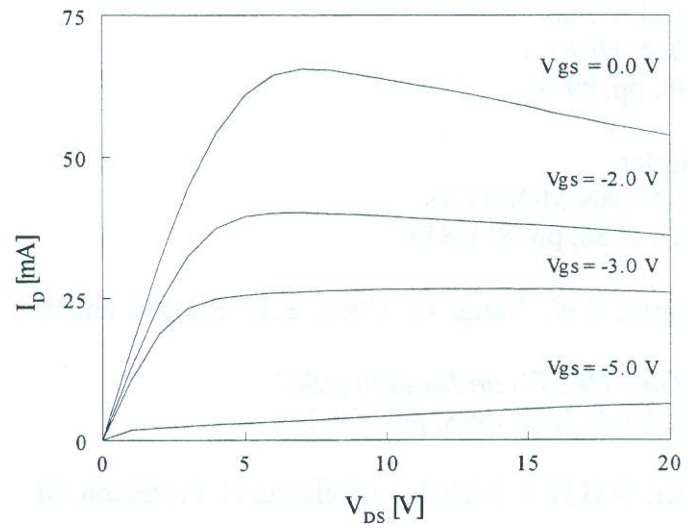

Figure 1b:
The drain-source current for a 160 μm wide transistor as function of drain-source voltage

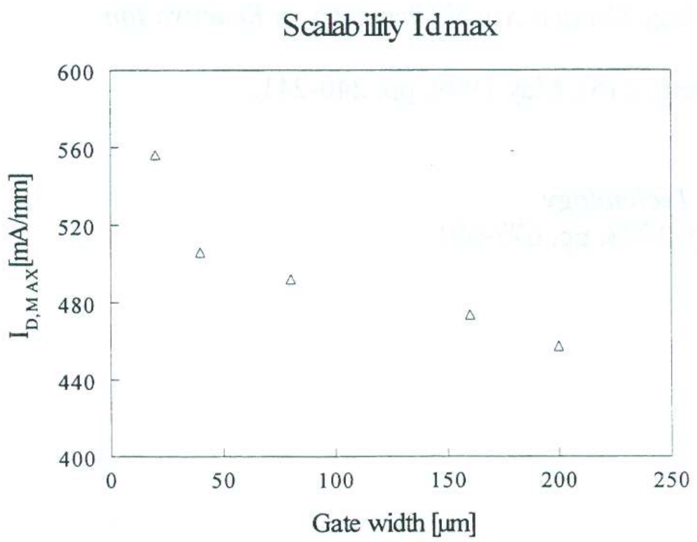

Figure 2a:
The scalability of the maximum drain-source current measured at V_{gs}=1.0 V

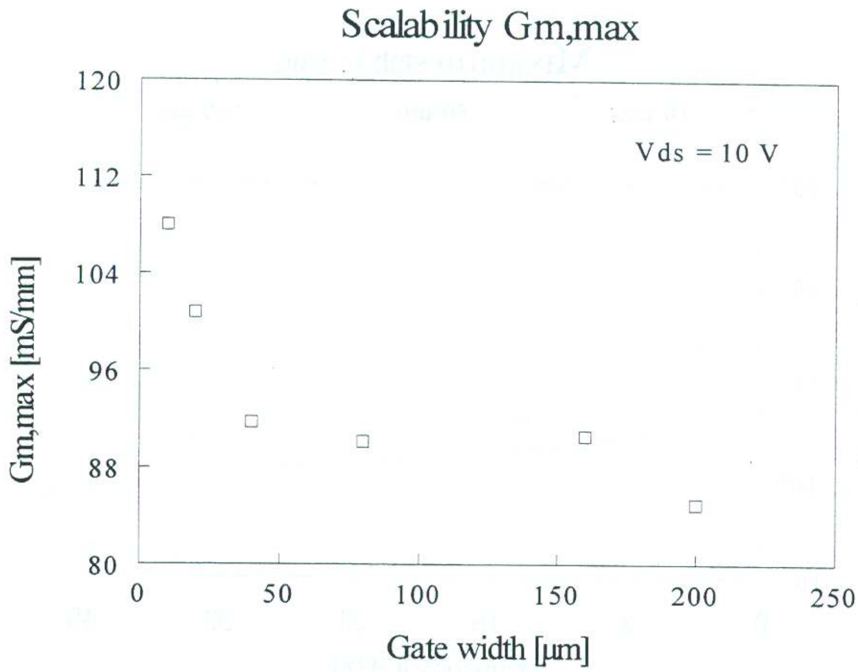

Figure 2b: Scalability of $G_{m,max}$ measured at V_{ds}=10 V

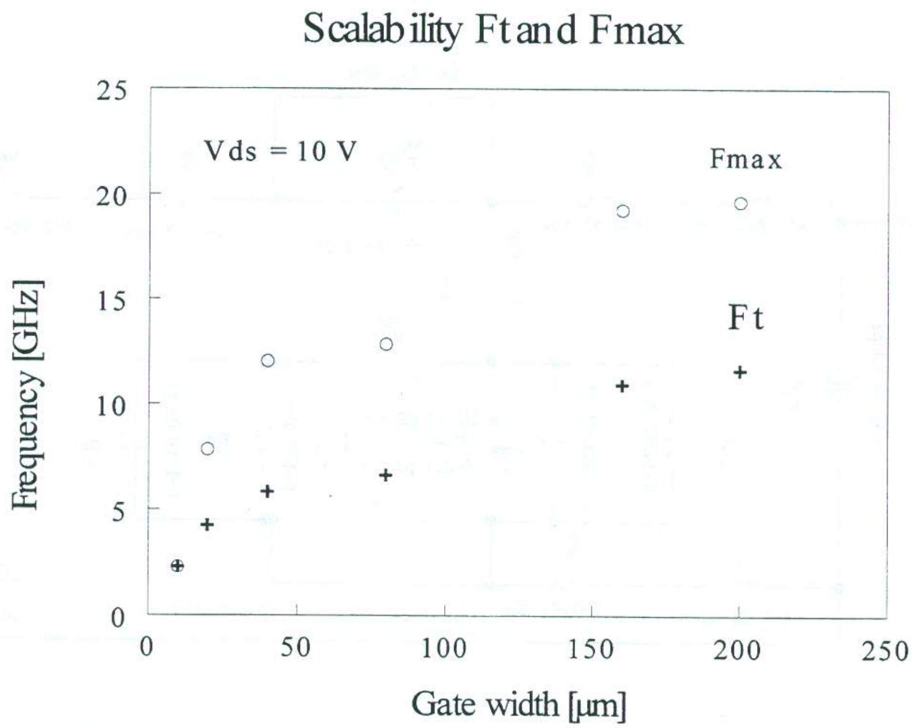

Figure 2c: Scalability of F_t and F_{max} measured at V_{ds}=10 V

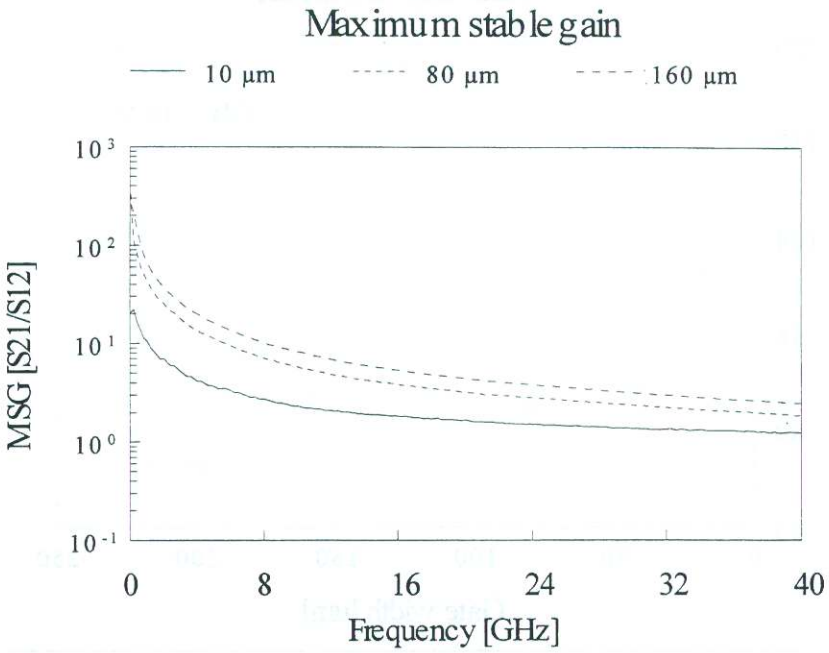

Figure 3: Maximum Stable Gain as a function of frequency for a 10, 80 and 160 µm wide transistor

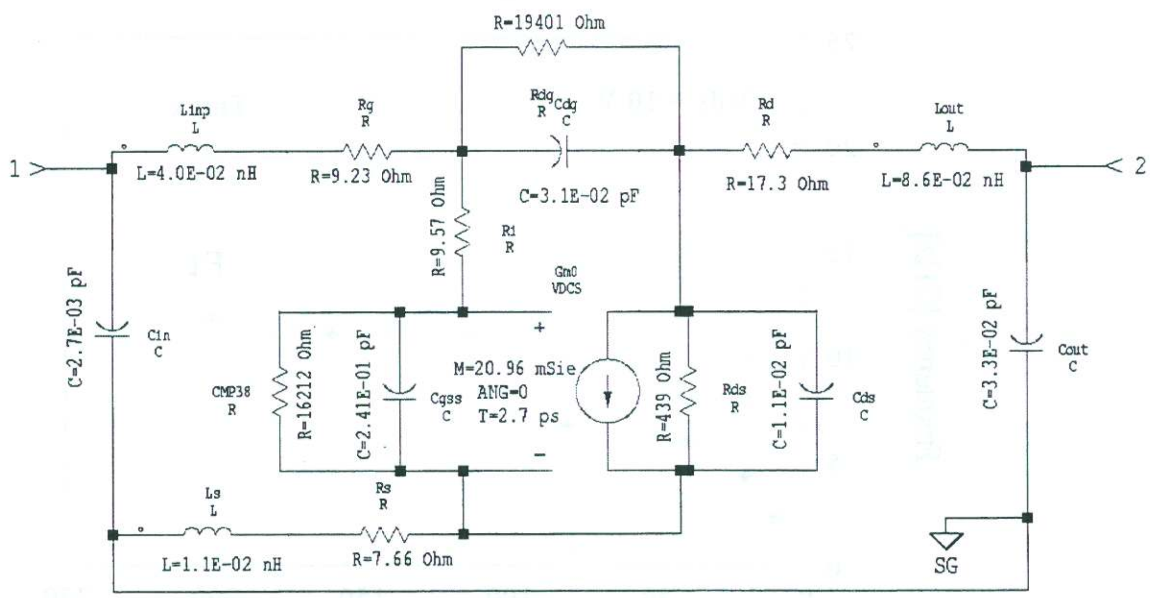

Figure 4: Small-signal equivalent circuit of a 200 µm wide transistor (V_{ds}=10 V and V_{gs}=-3 V)