PULSED MEASUREMENTS OF GaN MESFETs

B. Boudart, S. Trassaert, C. Gaquière, D. Théron and Y. Crosnier

Institut d'Électronique et de Microélectronique du Nord - DHS
U.M.R.-C.N.R.S. 8520- USTL - Avenue Poincaré - B.P.69
59652 VILLENEUVE D'ASCQ CEDEX – France
Tel : (33) 320197829 – Fax : (33) 320197888
Boudart@iemn.univ-lille1.fr

F. Huet and M. A. Poisson

Thomson C.S.F.-L.C.R.
91404 ORSAY France

Abstract - **GaN MESFETs were realized and then static and pulsed measurements were performed for two different lighting and temperature conditions. So, the existence of electrical traps associated with the surface states in GaN MESFETs was demonstrated. Hyperfrequency pulsed measurements were also performed to determine the maximum stable gain for different quiescent bias voltages and temperatures. This gain was found to increase with temperature.**

I. INTRODUCTION

The GaN material has outstanding electronic properties. This material was widely investigated for use in high power RF transistors [1-3]. The wider band gap (3.4 eV at room temperature) allows high supply voltages and high temperature applications [4,5]. But, up to now, all the devices electrical properties were not totally understood.

For these reasons a MESFET structure was chosen because it is easier to analyse than a HEMT structure. DC and pulsed measurements were performed to evidence the existence or not of electrical traps, their possible location, and their evolution with both the temperature and the light illumination. Furthermore, hyperfrequency pulsed measurements were performed to determine the maximum stable gain (MSG) for different quiescent bias voltages and temperatures.

First of all, the MESFETs technology is presented. Then DC and pulsed measurements of MESFETs are shown and analysed.

II. DEVICE PROCESSING

MESFETs were processed on epilayers grown by MOCVD on a (0001) sapphire substrate (Fig. 1). It consisted of a 250 Å GaN nucleation layer, a 3.6 µm GaN undoped layer and a 2000 Å Si-doped GaN active layer. A doping level of about 2.7 10^{17} cm^{-3} and a mobility of 330 cm^2/Vs were deduced from Hall measurements performed at room temperature.

Then, Ti/Al/Ni/Au (150/2200/400/500 Å) metallization layers were evaporated to realise ohmic contacts. These contacts were then annealed under nitrogen atmosphere at 900 °C during 30 s. The device isolation was made by reactive ion etching using 8 sccm of $SiCl_4$ gas, a rf power of 200 W and a pressure of 40 mTorr. This resulted in an etch rate of 200 Å/min. The gate length of 0.3 µm was defined by electron beam lithography. The metallization layers used for the Schottky contact were Pt/Au

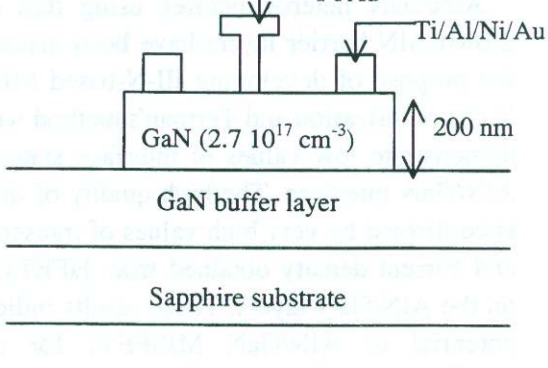

Figure 1 : GaN MESFET structure.

(100/1000 Å). The devices had a 2×50 μm wide gate and the source to drain spacing was 2.3 μm. The gate to source spacing was 1 μm. The analysed devices were not passivated.

III. DC MEASUREMENTS

Static I-V measurements are shown in Fig. 2 for two different lighting conditions. For a Vgs of 1 V and a Vds of18 V, the transistor exhibits a drain current of about 305 mA/mm with light and 270 mA/mm without light. This difference can be explained by the existence of electrical traps located in the material or/and at the surface. Further measurements were underway in order to determine their location.

IV. PULSED MEASUREMENTS

A. *Static Pulsed Measurements*

Pulsed measurements were also performed on the same device. Figure 3 exhibits the pulsed I-V characteristics with and without lighting for a quiescent bias voltage of Vds_0=18 V and Vgs_0=-9 V. The pulse widths used were 400 ns for Vgs and 380 ns for Vds. The trailing and leading edge were 50 ns. The frequency of the pulses was 100 kHz. In these conditions, the device can be considered as cold [6].

The maximum drain current is 120 mA/mm at Vds=18 V and Vgs=1 V without light, which is less than a half of the current obtained under static conditions. This loss confirms the presence of electrical traps. Indeed, under pulsed conditions, the DC bias origin was chosen in order

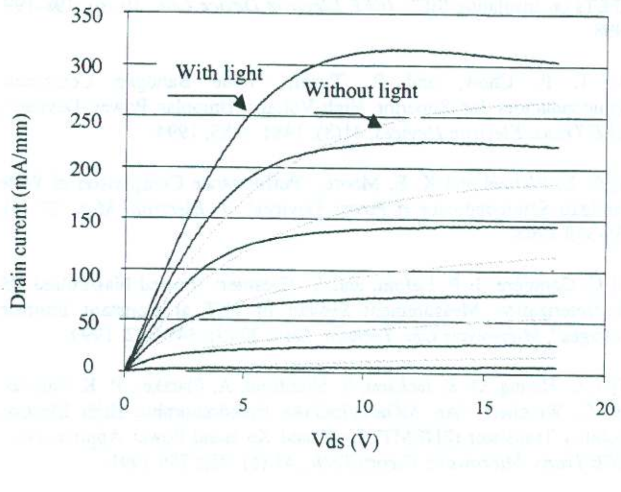

Figure 2 : DC I-V characteristics of a 2x50x0.3 μm^2 GaN MESFET with and without light for Vgs from –9 to 1 V (step 2 V).

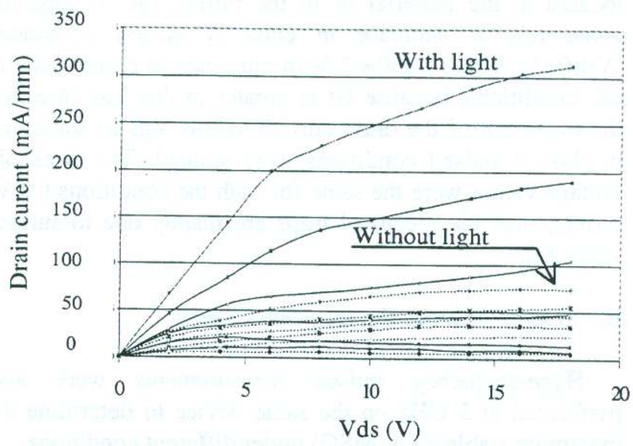

Figure 3 : pulsed I-V characteristics of a 2x50x0.3 μm^2 GaN MESFET with and without light for Vgs from –9 to 1 V (step 2 V).

to exalt the parasitic gating operated by the surface states.

The trap status corresponds to the quiescent bias point. So, in opposite to static conditions, the trapped electrons have not enough time to be in equilibrium at the instantaneous bias conditions as reported by Huang et al. [7]. Finally, the drain current obtained with light is nearly the same as under static conditions with light because electrons can be untrapped owing to the light.

In TABLE I, the drain current values obtained in different pulsed measurements conditions are summarised. By heating the device at a chuck temperature of 150 °C, the drain current is higher than at room temperature. For Vds0=18 V and Vgs0=-2 V, the current also increases due to the fact that the device is heated in these polarization conditions and the quiescent trap states are not the same.

All these different experiments prove the existence of electrical traps. Both the light and the temperature can untrap the trapped electrons which can then participate to the electrical conduction.

By comparing the evolution of the threshold voltage for the static and the pulsed characteristics, it is possible to locate the electrical traps in the device structure. Indeed, the expression of the threshold voltage Vt is given by :

$$Vt = Vbi - q\,(Nd + Nt)\,a^2 / 2\,\varepsilon$$

where Vbi, q, Nd, Nt, a and ε correspond to the built-in voltage, the electronic charge, the bulk doping, the trap density, the active layer thickness, and the dielectric constant, respectively. Then, if the electrical traps are

TABLE I : drain current evolution at Vgs=1 V for different measurements conditions.

Temperature	Vds0	Vgs0	Id at Vds=14 V
20 °C	18 V	-9 V	100 mA/mm
150 °C	18 V	-9 V	190 mA/mm
20 °C	18 V	-9 V	200 mA/mm

located in the material or in the buffer, the Vt absolute value has to decrease in class A pulsed conditions (Vds0=18 V and Vgs0=-2 V in our case) in comparison to DC conditions, because Nt is greater in this last case. So, the evolution of the drain current versus Vgs in static and in class A pulsed conditions were studied. The threshold voltage values were the same for both the conditions (-9 V) proving that the electrical traps are mainly due to surface states [7].

B. Hyperfrequency Pulsed Measurements

Hyperfrequency pulsed measurements were also performed at 3 GHz on the same device to determine the maximum stable gain (MSG) under different conditions.

The stimulus duration used in our experiments was 300 ns and the profile duration was 250 ns. The profile duration corresponds to the time the scattering parameters measurements are performed. The MSG was determined at Vds=10 V in three different conditions : the device was polarized in class A at room temperature, or in class B at room temperature, or in class B at a chuck temperature of 150 °C. Figure 4 shows the evolution of the MSG versus Vgs in these conditions. The MSG performed at room temperature and in class B is about 4 dB. The MSG obtained in class A at room temperature is 1 dB better than

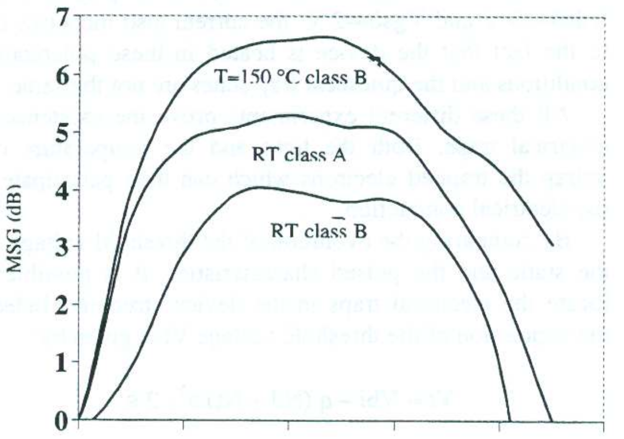

Figure 4 : evolution of the MSG performed by hyperfrequency pulsed measurements at 3 GHz versus Vgs at Vds=10 V in different conditions.

the first one. In fact, in these conditions the device is hotter and the surface trap states are lower [7]. The MSG obtained at a chuck temperature of 150 °C in class B is better again than the first two. So, the MSG improves by heating internally or externally the device.

V. CONCLUSION

Electrical traps were evidenced in GaN MESFETs by DC and pulsed measurements performed under several conditions (with or without light, with or without heating). These electrical traps, associated with the surface states, degrade the device performances at low temperature. But, the electrical performances of GaN MESFETs are improved by heating the device. Then GaN material is a good candidate for power and high temperature applications.

VI. ACKNOWLEDGEMENT

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