A New Empirical Non-linear Model for SOI MOSFET

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Abstract – An empirical non-linear model for SOI MOSFET useful for large-signal simulations of high frequency circuit design is presented. An original close form expression is proposed for the drain current and charge conservation is taken into account, as capacitances are derived from a single charge model. The model's parameters are first extracted, prior the model implementation in a circuit simulator. Then some comparisons with experimental data are proposed to validate the model. Note that the model is well suited for the Fully Depleted either the Partially Depleted devices.

INTRODUCTION

SOI MOSFET devices present more and more interesting high frequency performances along with the continuous decrease of the gate length. For this reason, it seems realistic to use such devices in centimetric and probably millimetrique wave ranges [1] [3].

Several empirical non-linear models for MESFET's and HEMT's have been developed for high frequency applications, but not so much for MOSFET on SOI substrate. The existing ones are generally physics oriented and they require technological data for their parameter extraction [2].

The aim of this paper is to present an empirical non-linear model for SOI MOSFET, easy to extract, scalable on gate width, for applications like amplifiers, mixers and oscillators down to the millimetrique range. This model, which was studied for Fully Depleted (F.D.) and Partially Depleted (P.D.) SOI MOSFET's realised by the CEA LETI [3], describes accurately their electrical (DC-AC) characteristics. It includes a non-linear drain current expression that is continuous and infinitely derivable, leading the transconductance and the drain conductance to be continuous. The capacitances are derived directly from a single charge model. The model's parameters are first extracted, prior the introduction, as capacitances are derived from a single charge model. The model is well suited for the Fully Depleted either the Partially Depleted devices.

THE NON LINEAR DRAIN CURRENT

The drain current equation is originally based on the Angelov's [4] model developed for III-V devices, but it has been modified in order to be suitable for SOI devices:

\[ I_{dsi}(V_{gsi}, V_{dsi}) = Kf(V_{gsi})f(V_{gsi}, V_{dsi}) \]  

In (1), the first function depends on the control voltage \( V_{gsi} \) while the second one is dependent on both \( V_{gsi} \) and \( V_{dsi} \). More specifically the drain current is given by the following expression:

\[ I_{dsi}(V_{gsi}, V_{dsi}) = I_{pk}Wf_{n}f_{f} + p(V_{gsi})\tanh(V_{gsi}) \]

\[ \psi(V_{gsi}) = p(V_{gsi}) \tan(V_{gsi}) + K_{1}V_{gsi} + \alpha \]

\[ p(V_{gsi}) = K_{0} + K_{1}V_{gsi} + K_{2}V_{gsi}^{2} + K_{3}V_{gsi}^{3} \]

\[ \psi(V_{gsi}) = 1 + K_{1}V_{gsi} + K_{2}V_{gsi}^{2} + K_{3}V_{gsi}^{3} \]

In (2) \( \psi \) is the same term as those used in Angelov model [4]. Polynomial expressions were added to better describe the experimental variations of the transconductance \( g_{m} \) and conductance \( g_{d} \) in the saturation regime. The term \( \tanh(V_{dsi}(K_{0}V_{gsi} + \alpha)) \) describes the region between the linear and the saturation regime of the transistors. The last term ensures a current to be equal to zero in subthreshold region and for negative gate biases. All the terms \( P_{1}, K, \alpha, V_{pk} \) and \( I_{pk} \) are the current model's parameters, \( W \) is the transistor's width per finger and \( n_{f} \) the number of fingers. \( V_{th} \) is the measured threshold voltage. They don't have any real physical meaning (except of \( V_{th} \)) even if some of them have physical dimensions.

The transconductance's and conductance's equations are given by:

\[ g_{m} = \frac{1}{2} \frac{1}{R_{s}} \]
\[
g_{ds}(V_{gs}, V_{ds}) = \frac{dI_{ds}}{dV_{ds}} \bigg|_{V_{ds} = \text{sat}} \tag{3}
\]
\[
g_{ds}(V_{gs}, V_{ds}) = \frac{dI_{ds}}{dV_{ds}} \bigg|_{V_{ds} = \text{sat}} \tag{5}
\]

This model describes the static current versus the intrinsic voltages \(V_{gs}\) and \(V_{ds}\), taking into account the potential drop across \(R_s\) and \(R_d\).

**THE NON LINEAR CAPACITANCE**

The best way to model capacitance and to keep charge conservation is to consider the total charge at a given physical point of a device [5]. The charge on the gate electrode depends on the gate bias and the drain bias: \(Q_d(V_{gs}, V_{ds})\). The capacitance \(C_{gs}\) and \(C_{gd}\) will be [5]:

\[
C_{gs} + C_{gd} = \frac{dQ_d}{dV_{gs}} \bigg|_{V_{ds} = \text{sat}} \tag{4}
\]

The capacitances \(C_{gs}\) and \(C_{gd}\) are derived from the same charge expression and are interdependent. They have to verify this mathematical relation (4), otherwise the model is not charge conservative. Using a charge model from which the expressions for \(C_{gs}\) and \(C_{gd}\) are calculated by (4), we can model the gate capacitances without having to take into account of a transcapacitance \(C_m\) element [5], [6].

Following this principles the gate charge for the MOS SOI transistors was modelled by the equation inspired by [7]:

\[
Q_d = K \left( f_1(V_{gs}, V_{ds}) + f_2(V_{gs}, V_{ds}) \right)
\]

\[
K = C_{gs}W_f \left( L_g - 2L_g \right)
\]

\[
f_1 = \left( C_{gs}V_{gs} + C_{gs}V_{gs}^2 + C_{gs}V_{gs}^3 \right) \left( V_{gs0} + \tanh \left( \frac{V_{ds}}{2V_{th}} \right) \right) \tag{5}
\]

In (5), \(L_g\) is the gate length, \(W_f\) the gate width per finger and \(n_f\) the number of fingers. \(C_{gs}, L_g, C_{gs}, C_{gd}\), \(\gamma\) and \(V_{th}\) are the model parameters. (4) and (5) give the explicit functions for \(C_{gs}\) and \(C_{gd}\).

**SIMULATION, RESULTS**

We present here the results obtained for a FD SOI MOSFET with \(W=8x12.5\ \mu m\), \(L_g=0.25\ \mu m\) and with salicide gate. The model parameters extracted for this transistor are summarized in table I.

The parameters were extracted using an optimisation procedure in the ICCAP environment (Agilent Technologies EESof), by adjusting the model equations on the measured DC and AC data. The intrinsic and extrinsic elements were deduced from bias depending S-parameter measurements [8]. The model was implemented in the ADS (Agilent Technologies EESof) circuit simulator. Small signal and large signal simulations were carried out in order to perform some comparisons with experimental data and validate the model.

![Fig. 2a Static drain current versus drain bias for 5 different values of gate bias. Measurements (symbols) and model (solid line).](image)

![Fig. 2b Static transconductance gm versus gate bias Vgs for Vds=1V. Measurements (triangles) and model (solid line). Static conductance gd versus drain bias Vds for Vgs=1V. Measurements (circles) and model (solid line).](image)

We observe an excellent agreement in Fig.2a-b upon the static simulation for the drain current versus \(V_{ds}\) for different values of \(V_{gs}\), but also for the output conductance \(g_d\) and the transconductance \(g_m\). In Fig.3 is shown the capacitance \(C_{gd}\) measured and modelled by the expressions (4) and (5). There is a slight disagreement due to the fact
that, a priori, we don’t know the exact expression of the gate charge, nevertheless the model is charge conservative.

\[ C_{gs}(F) = f(V_{gs}) \]

Fig. 3. Capacitance $C_{gs}$ versus gate bias $V_{gs}$ for $V_{ds}=0, 1$ and $2$ V. Measurements (symbols) and model (solid line).

Next, in Fig.4 a-b, the small-signal simulations are compared to the measured ones. The four S-parameters are plotted for frequencies varying from $0.25$ GHz to $50$ GHz and the agreement is quite good.

\[ S_{22}, S_{11}, S_{21}, S_{12} \times 10 \]

Fig. 4.a $S_{11}$ and $S_{22}$ parameters versus frequency varying from $0.25$ GHz to $50$ GHz for $V_{gs}=0.6$ V and $V_{ds}=1$ V. Measurements (symbols) and model (solid line).

\[ S_{21}, S_{12} \times 10 \]

Fig. 4.b $S_{21}$ and $S_{12}(x10)$ parameters versus frequency varying from $0.25$ GHz to $50$ GHz for $V_{gs}=0.6$ V and $V_{ds}=1$ V. Measurements (symbols) and model (solid line).

Finally, in order to validate the model, some large signal measurements have been carried out. For this purpose, we have applied at the input of the device a microwave power $P_{in}$ using a $50 \, \Omega$ generator and measured the output power $P_{out}$ absorbed by the $50 \, \Omega$ load (Fig.5) [9]. The results are shown in Fig.6.a and a good agreement has been observed with the large signal simulation made using ADS.

\[ P_{out} \]

Fig. 5 Schematic measurement setup used for determination of the one tone power response of the device.

\[ P_{out}, P_{in}, \text{Gain} \]

Fig. 6.a Output power $P_{out}$ and gain versus input power on the transistor with $W=8x12.5 \, \mu m$, $f=4$ GHz, $V_{gs}=1.5$ V, $V_{ds}=2$ V. Measurements (symbols) and model (solid line).

The scalability of the model in large signal condition versus gate width $W$ has been checked as well on Fig.6.b, where we present the $P_{out}$ versus $P_{in}$ of the transistor with $W=8x12.5 \, \mu m$ scaled at $W=8x6.25 \, \mu m$, and we compare it to the measured data of a transistor with $W=8x6.25 \, \mu m$ (same frequency and biases).

\[ P_{out}, P_{in}, \text{Gain} \]

Fig. 6.b Output power $P_{out}$ and gain versus input power on the transistor. Measurements (symbols) and model (solid line).

CONCLUSIONS

In this paper a new empirical non-linear model for SOI MOSFET’s (FD and PD) has been presented. This model is based both upon close form expressions of the non-linear drain current and gate charge. The parameters of the model can be easily extracted using ICCAP optimiser and the comparisons in terms of static and dynamic performances
are in good agreement with the experimental ones. Finally, single tone large signal measurements have been made and compared with simulations. As a conclusion, this non-linear model can be useful for the design of centimetric and millimetric non-linear circuits (mixers or oscillators).

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REFERENCES


