25W L-BAND POWER MODULE FOR SPACE APPLICATIONS

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ABSTRACT **- A high efficient, low distortion L-band power module using a linear and non-linear models of the HFET devices has been developed.**

Single stage hybrid amplifier fabricated with 4x18mm gate width HFET exhibits an output power of 43.8dBm, a linear gain of 17dB and an associated PAE of 60% at 1.5GHz.
These excellent results are performed by developing an accurate non-linear model of the chip device and optimizing the matching networks of the amplifier.

I. *INTRODUCTION*

High efficiency and low distortion power amplifiers are a vital requirement in communication satellites. These extremely reliable elements at L and S-band are necessary to satisfy the increasing demand for navigation and GPS payload [1] .
HFET and PHEMT devices are becoming a very attractive choice for use in microwave power amplifiers due to specific characteristics such as high gain, linearity and high output power [2] [3] [4].
In this paper, we present the results of a power module at L-band achieving an output power of 43.8dBm, a linear gain of 17dB with an associated Power Added Efficiency (PAE) of 60%.

II. *POWER MODULE DESIGN*

Power modules are difficult to develop due to inadequacy measurements to characterise large periphery devices.
To overcome this problem, a comprehensive methodology is employed in this design using the scaling method [5]. A small cell of 4.8mm periphery is characterised with small-signal {S} parameters measurements and DC pulse tests. This measurements allow to extract the electrical parameters of linear and non-linear models. General rules of scaling are used in order to obtain the electrical model parameters of power HFET device used in the power module.
In this way, an hybrid power module is designed using four high power discrete 0.5µm HFET devices connected in parallel (18mm gate widths from Triquint Semiconductor Texas).
Non-linear model of the HFET device is biased at class AB with Drain voltage of Vds=7volts and optimum loads at the fundamental and the second harmonic signal are determinated from simulated load-pull method [6] [7] [8].
Then, the matching networks of the power module are optimized by the harmonic balance simulator (Libra of HP-Eesof) to achieve the optimum combination of high output power and high PAE.

The input and output matching networks are designed on a high relative dielectric constant material (ε_r=38), in order to reduce significantly the size of the module.
The RF and DC decoupling as well as the bias circuits are included in the power module to make it a self-content amplifier without the need of outside circuitry.
The simulated AM/AM response of the power module for a single carrier (Vds= 7V, class AB) is shown in figure 1. The output power is higher than 43.8 dBm, with the associated PAE greater than 60% (including the insertion losses of the test jig and the SMA connectors).

Figure 2 presents the load cycle at the output port of one of the 18mm chip devices. The area of this I-V curve is minimum corresponding to a minimum power consumption.

The unconditional stability of the power module was checked by the K-factor analysis. The non existence of odd mode oscillations and the parasitic loops were checked by using the Normalized Determinant

Function (NDF) method over the frequency range from 0 to 20 GHz [9] [10]. Figure 3 shows the corresponding real and the imaginary parts of the NDF factor over the frequency range from 0 to 25 GHz. This amplifier is stable since the locus of the NDF does not encircle the origin (0,0). The gain margin for the stability is greater than 40 dB from 0 to 8 GHz.

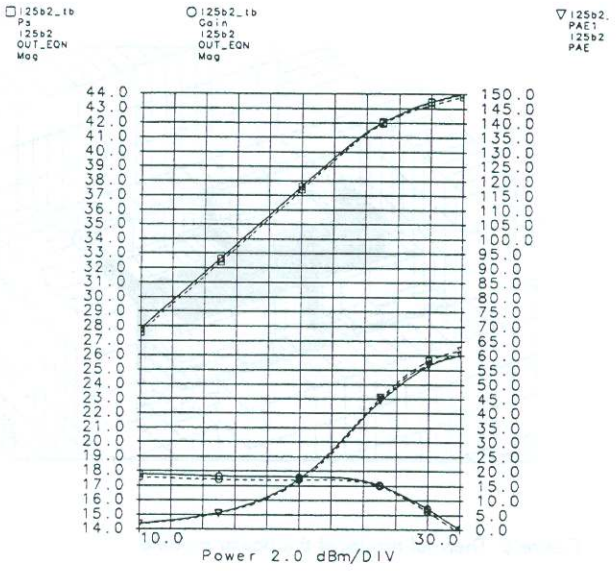

FIGURE 1: Simulated output power, gain, and power-added efficiency versus input power of the HPA at V_d=7V (1.45-1.55GHz).

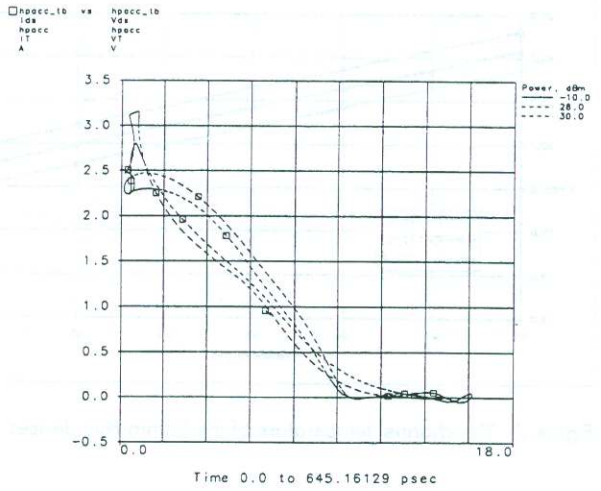

FIGURE 2: Load cycle at the output port of the 18mm device at 1.5GHz for the total input power of -10dBm,28dBm and 30dBm .

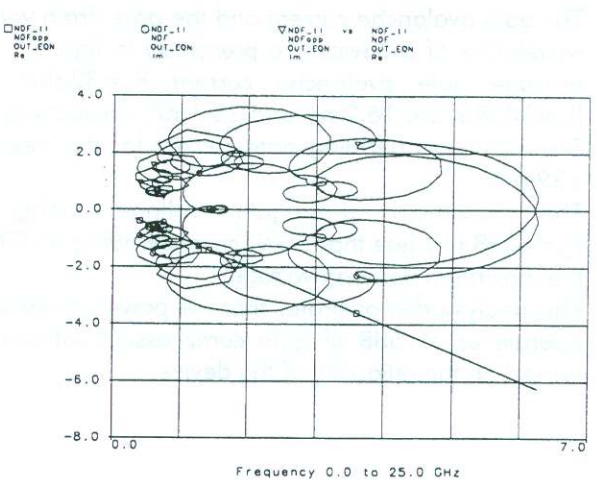

FIGURE 3: The real and the imaginary parts of the NDF factor over the frequency range from 0 to 25 GHz.

Mastering the non-linear model allows to simulate the instantaneous non-linear gate forward current and gate-drain breakdown voltage to check that the power module is designed in a safe operating area. Because of reliability is of extremely high importance for space application, this methodology is a main advantage over the more classical approach based on life test data only.

Figure 4 shows the forward gate current and gate voltage waveforms of a device for two levels of input power: 32dBm (3.5dB of gain compression) and 34dBm (5.5dB of gain compression).

The average forward gate current for P_{in}=32dBm and P_{in}=34dBm are 17.7mA and 42.1mA, respectively.

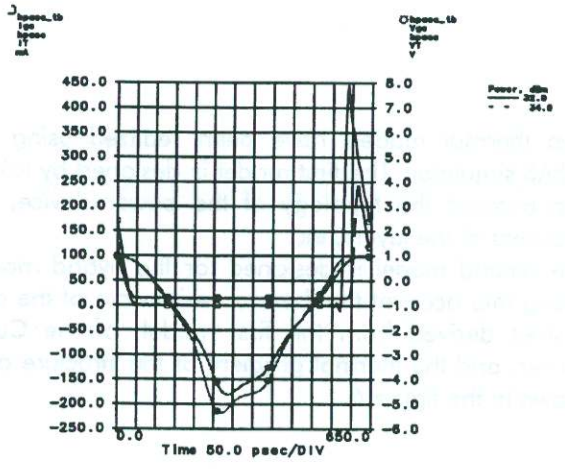

FIGURE 4: the forward gate current and gate voltage waveforms for: P_{in}=32dBm (3.5dB of gain compression) and P_{in}=34dBm (5.5dB of gain compression), f=1.5GHz.

The gate avalanche current and the gate-drain voltage waveforms of a device are presented in figure 5. The average gate avalanche current P_{in}=32dBm and P_{in}=34dBm are 16.2mA and 25.1mA, respectively.
The maximum derating gate current for this device is ±39mA.
The maximum drain-gate voltage swing for P_{in}=34dBm is less than 22V, corresponding to 70% of the maximum derating voltage.
This analyse demonstrates that the power module can operate up to 5dB of gain compression without any impact on the reliability of the device.

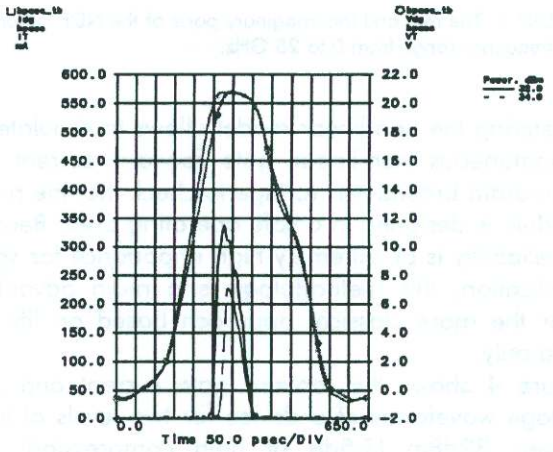

FIGURE 5: the avalanche gate current and gate-drain voltage waveforms for: P_{in}=32dBm (3.5dB of gain compression) and P_{in}=34dBm (5.5dB of gain compression) , f=1.5GHz.

Two thermal models have been realized using the IDEAS simulator. The first model is designed by taking into account the topology of the power device, the thickness of the layers, etc.
The second model is designed for the hybrid model, taking into account the thermal resistances of the chip devices derived from the first model, of the Cu/W carrier, and the thermal gradient of the structure as is shown in the figure 6.

The simulated dissipated powers as a function of reference temperature (Tref) for three values of channel temperature (Tj) are given in the figure 7. The dissipated power for the channel temperature of 115°C is 24W for the reference temperature of 55°C.

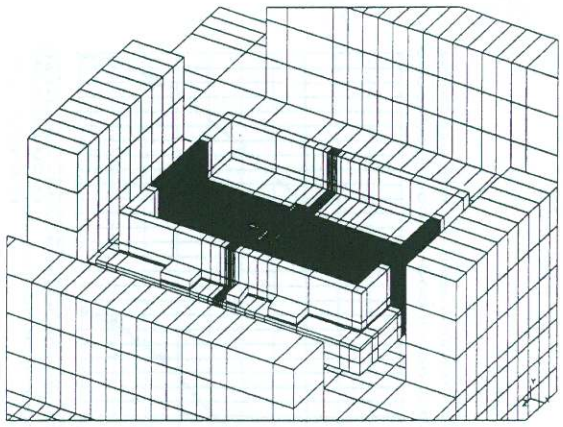

Figure 6: Thermal model of the power module

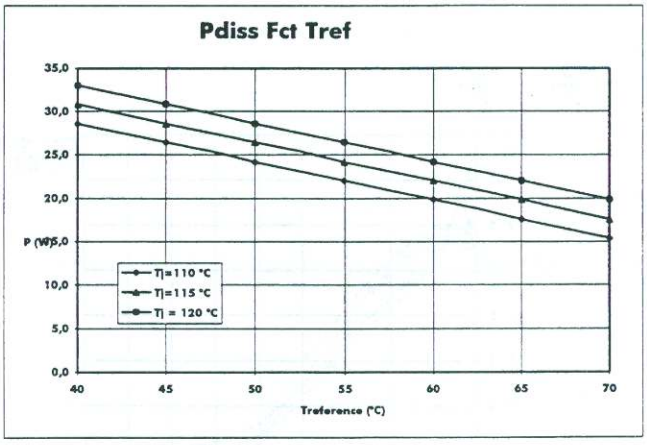

Figure 7 : The channel temperature of the 18mm chip devices

III. EXPERIMENTAL RESULTS

The measured results of the power module under CW signal excitation in class A/B operation, at Vds= 7V is given in figure 8. The output power is higher than 43.8dBm, with the associated power added efficiency of 60% at 1.5GHz (including the insertion loss of the test jig and the SMA connectors).
The measured results of the power module such as P_{out} and PAE agree very well with the simulated results as are shown in the figures 1 and 8.

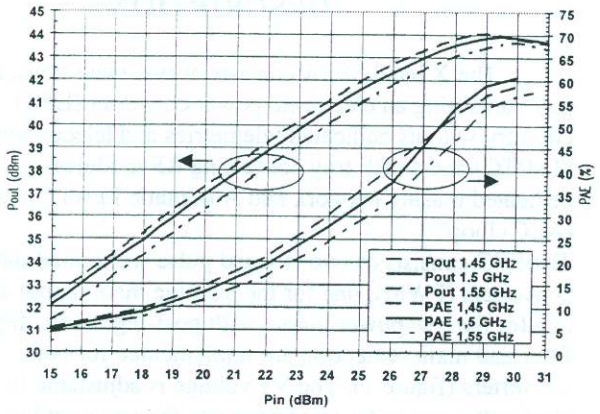

Figure 8 : Measured output power, and power-added efficiency versus input power of the HPA at V_d=7V.

IV. CONCLUSION

The use of power HFET devices and hybrid technology allow to achieve the best output power and PAE with good linearity and to minimize the weight and the size of the SSPA.
Using the comprehensive methodology developed by Alcatel Space Industries, linear and non-linear electrical models of HFET chip devices were established. This work has allowed us to design a power module at L-band for space application.

V. ACKNOWLEDGMENTS

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VI. REFERENCES

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