A UNIFIED APPROACH TO HIGH EFFICIENCY MICROWAVE POWER AMPLIFIER DESIGN

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Abstract - **A systematic approach to the design of high efficiency microwave power amplifiers is presented. The technique makes use of second and third harmonic terminating idlers to achieve major improvements in output power, gain and power added efficiency. The approach proposed in this contribution is validated by means of a sample design and realisation, illustrating both the effectiveness and the feasibility of the method, as compared to more conventional harmonic tuning strategies.**

I. INTRODUCTION

High efficiency power amplifier design is indeed one of the major concerns of the microwave designer. The power stage is in fact a critical part in many subsystems, ranging from commercial mobile telephone applications to satellite payloads, microwave transponders and many others. The key feature requested to the power stage is minimum power consumption, that is basically translated in the minimisation of the number of battery cells, reduction of heatsink dimensions and therefore in the minimum size and weight of the entire microwave unit. This task can be accomplished making use of appropriate design techniques, targeted to high efficiency and low voltage operation of the microwave power stage.

Different techniques have been proposed in the past to fulfill such tight constraints [1], many of them utilising the harmonic tuning of the voltage and current output waveforms [2, 3], in order to optimise the power performances of the amplifying stage. On the other hand, such approaches have focused on even / odd harmonic terminating schemes [4], not accounting for the difficulties arising from their practical microwave implementation, or limited their target to the control of a single harmonic component [5].

In the following, a comprehensive approach will be attempted, taking into account the second and third harmonic components of the output waveforms. Their generation and control will be discussed, together with the theoretical improvements in power performances arising from their manipulation.

A practical design example will be illustrated, demonstrating, by means of a full nonlinear device model and analysis method, that a careful and guided choice of input and output harmonic loading may lead to dramatic improvements in the output power, large signal gain and power added efficiency of a power amplifying stage.

II. DESIGN ASSUMPTIONS AND VOLTAGE WAVESHAPING

As previously noted, the number of harmonics that can be effectively controlled is limited by two major constraints: firstly, the complexity of the resulting circuit, impacting both the die size and yield; secondly, as harmonic order (and frequency) increases, the proper modelling of the passive and active components used becomes increasingly difficult: as a consequence, the design of the circuit idlers necessary to realise harmonic terminations is less accurate and therefore less effective.

From the practical point of view, the controllable harmonic components are restricted to the first three ones (namely the fundamental, second and third harmonic) and the harmonic manipulation procedure itself must take into account such fundamental limitation.

The fundamental limitation in power performances of an amplifying stage arises from the physical constraints imposed on drain current and voltage swings by the device gate-source breakdown, the ohmic region, input junction forward conduction and channel pinch-off.

For low-voltage high efficiency power amplifier design, the main limitation is the device ohmic region, constraining the drain voltage to values higher than the device knee voltage V_k. For a given drain bias point $V_{ds,dc}$ a maximum fundamental frequency voltage amplitude $V_{ds,1,max}=V_{ds,dc}-V_k$ is therefore allowed by design techniques not introducing a harmonic manipulation.

The idea underlying harmonic manipulation is the proper shaping of the drain voltage waveform so to obtain an higher fundamental frequency amplitude. More in detail, if the voltage waveform is flattened while approaching the device ohmic region by means of properly phased second and third harmonic components, its minimum value is accordingly increased for a given fundamental frequency component. Such increase actually

allows a corresponding increase in the fundamental-frequency voltage component, that in the limiting case may be selected such that the resulting flattened voltage waveform reaches the ohmic region physical limitation. The resulting fundamental frequency voltage component can be made much higher, increasing accordingly output power, gain and power-added efficiency of the stage.

The increase in the fundamental voltage component may be obtained in two different ways: for a given drive level (and therefore drain current waveform), the fundamental frequency drain load may be increased from the previous value, therefore determining, together with the fundamental frequency drain current component, the corresponding drain voltage. Alternatively, for a given drain load, the drive level may be increased, therefore allowing an higher compression point (and therefore higher linearity) for the amplifying stage. For optimum output power and efficiency performances however, the first approach must be chosen.

The complete analysis of the problem will not be presented in this contribution for the sake of brevity, but the fundamental results will be shown.

If the drain voltage waveform is expressed as the sum of a dc ($V_{ds,dc}$), fundamental ($V_{ds,1}$), second ($V_{ds,2}$) and third harmonic ($V_{ds,3}$) components,

$$V_{ds}(\vartheta) = V_{ds,dc} - V_{ds,1}\cdot\cos(\vartheta) - V_{ds,2}\cdot\cos(2\vartheta) - V_{ds,3}\cdot\cos(3\vartheta) \quad \text{where} \quad \vartheta = \omega t \tag{1}$$

a "Voltage Gain Function", $\delta(k_2,k_3)$, can be introduced, defined as the increase in fundamental frequency voltage component over the unmanipulated one:

$$\delta(k_2,k_3) \equiv \frac{V_{ds,1}}{V_{ds,1,max}} = \frac{-1}{\min_{\vartheta}\left[V_{ds}(\vartheta,k_2,k_3)\right]} \tag{2}$$

$$\text{where} \quad k_2 \equiv \frac{V_{ds,2}}{V_{ds,1}} \quad \text{and} \quad k_3 \equiv \frac{V_{ds,3}}{V_{ds,1}}$$

It is to note that the phase relationship between fundamental and harmonic components (reflected in the sign of the k_2 and k_3 coefficients) must be properly selected, in order to flatten the voltage waveform while it approaches the physical limitation. Such effect is depicted in fig.1, where the two cases of proper and erroneously phased components are shown.

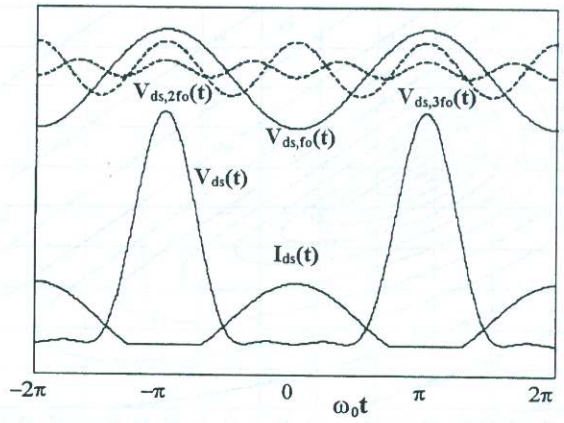

Fig.1a: Typical drain voltage waveform as composed by properly phased harmonic components

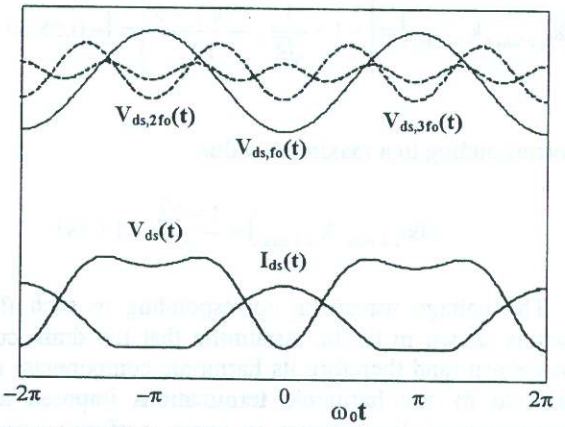

Fig.1b: Typical drain voltage waveform as composed by harmonic components with a wrong phase relationship

If proper second and third harmonic terminations are employed, the same voltage swing of the unmanipulated waveform can be obtained but with an higher fundamental-frequency component, i.e.:

$$V_1\big|_{HM} = \delta(k_2,k_3)\cdot V_{ds,1,max} \tag{3}$$

Such higher fundamental frequency amplitude can be obtained, at the same input drive level, simply loading the device with a termination given by:

$$Z_{HM,1} = Z_{TL}\cdot\delta(k_2,k_3) \tag{4}$$

where Z_{TL} is the load at fundamental frequency in the unmanipulated case.

The contour plot of the voltage gain function in the plane (k_2,k_3) is shown in fig.2, exhibiting an absolute maximum for

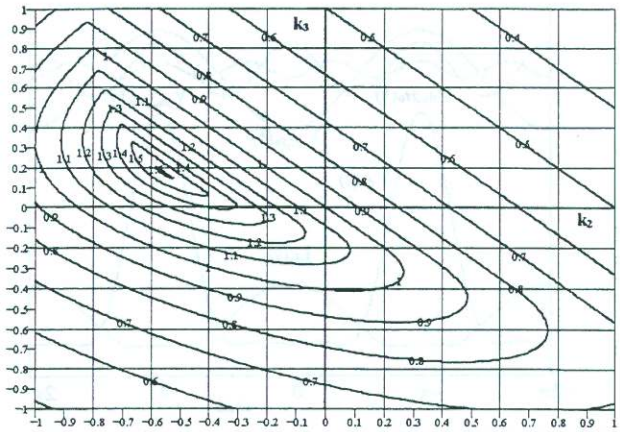

Fig.2: Contour plot of the voltage gain function in the k_2, k_3 plane

$$\left[k_{2,\delta\max}, k_{3,\delta\max}\right] = \left[-1+\frac{1}{\sqrt{5}}, \frac{3\cdot\sqrt{5}-5}{10}\right] = \left[-0.553, 0.171\right] \tag{5}$$

corresponding to a maximum value

$$\delta\left(k_{2,\delta\max}, k_{3,\delta\max}\right) = \frac{1+\sqrt{5}}{2} = 1.6181 \tag{6}$$

The voltage waveform corresponding to such ($\mathbf{k_2}$,$\mathbf{k_3}$) pair is shown in fig.1a. Assuming that the drain current waveform (and therefore its harmonic components) is not affected by the harmonic terminations imposed at the device output, the increase in power performances from the unmanipulated case will be given by:

$$P_{out,HM} = P_{out,TL} \cdot \delta(k_2, k_3) \tag{7a}$$

$$G_{HM} = G_{TL} \cdot \delta(k_2, k_3) \tag{7b}$$

$$\eta_{d,HM} = \eta_{d,TL} \cdot \delta(k_2, k_3) \tag{7c}$$

Thus, a theoretical maximum improvement of 62% in output power, gain and drain efficiency over the unmanipulated design approach can be expected.

On the other hand, the use of even order harmonic components (in this case the second one) actually flattens the voltage waveform toward while approaching the ohmic limitation and peaks it towards device breakdown. This effect must be carefully evaluated, since it may lead to a decrease in power performances arising from the onset of the device breakdown. Quantitatively, a "Voltage Overshoot Function", $\beta(\mathbf{k_2},\mathbf{k_3})$ may be defined as

$$\beta(k_2, k_3) \equiv \frac{\max_\vartheta\left[V_{ds,norm}(\vartheta)\right]}{\max_\vartheta\left[V_{ds,denormalised}(\vartheta)\right]} = \max_\vartheta\left[V_{ds,norm}(\vartheta)\right]\cdot\delta(k_2, k_3) \tag{8}$$

and the corresponding contour plot is shown on fig.3.

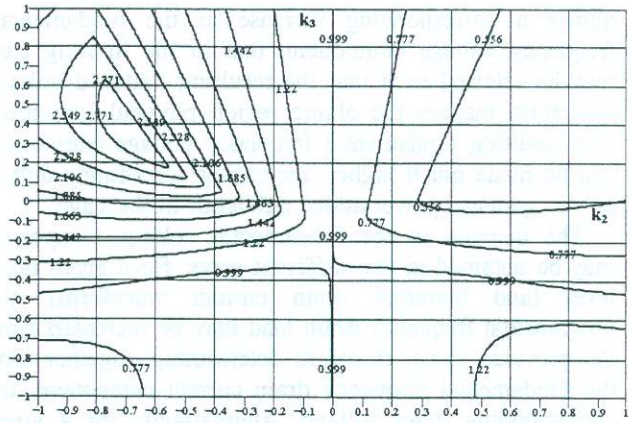

Fig.3: Contour plot of the voltage overshoot function in the k_2, k_3 plane

As it can be easily noted from the signs of the optimum $\mathbf{k_2}$ and $\mathbf{k_3}$, the second and third harmonic components must be properly phased with the fundamental one. Since only passive terminations can be employed, this consideration in turn implies that they have to be present, with the correct phase, already in the drain current waveform:

$$V_{ds,k} = Z_{d,k} \cdot I_{d,k} \qquad k = 2,3... \tag{8}$$

This task can be accomplished utilising both input and output terminating impedances at second and third harmonic, therefore accounting also for the input nonlinearities [6] of the device (mainly the gate-source capacitive one).

III. SAMPLE DESIGN AND RESULTS

To demonstrate the feasibility of the approach, a single-stage power amplifier has been designed making use of a full nonlinear device model and CAD package. The device is a medium power MESFET from Alenia Marconi Systems, and its nonlinear model has been extracted using pulsed dc and multibias S-parameter measurements. A companion stage, for comparison purposes, has been designed with a conventional tuned load approach. The simulated results are summarised in the table I and II, where the performances of the two stages are compared at 1 dB compression and at maximum efficiency drive levels respectively.

TABLE I	P_{in}=14.5 dBm (1dB compression)	
	Tuned Load	Harmonic Manipulation
P_{out} [dBm]	23.4	24.3
PAE [%]	37.8	55.1

TABLE II	P_{in}=17 dBm (max PAE)	
	Tuned Load	Harmonic Manipulation
P_{out} [dBm]	23.9	25.3
PAE [%]	36.5	60.6

To demonstrate the effect of the harmonic manipulation on the load curve (i.e. the instantaneous plot of drain current and voltage superimposed on the device output characteristics), in fig.4 the simulated load curve corresponding to the 1dB compression point is plotted.

Finally, in fig. 5 and 6 are reported the output power and the power-added efficiency obtained from the two hybrid power amplifiers realised at Alenia Marconi Systems. The experimental results, obtained without any additional external tuning, clearly demonstrate the effectiveness of the proposed design approach stressing the dramatic improvement in power-added efficiency.

IV. CONCLUSIONS

A unified approach for the design of low-voltage high-efficiency power amplifier with the harmonic manipulation approach has been presented. A low-voltage amplifier design has been performed and compared to a standard design, demonstrating the remarkable improvements that can be obtained by means of the harmonic manipulation strategy.

ACKNOWLEDGMENTS

The Advanced Research Technology Group of Alenia Marconi Systems is deeply acknowledged for their support in realising the amplifiers and performing the measurements.

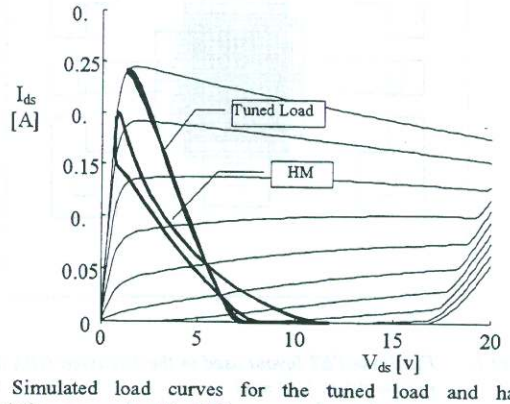

Fig.4: Simulated load curves for the tuned load and harmonic manipulation approach at the 1dB compression point.

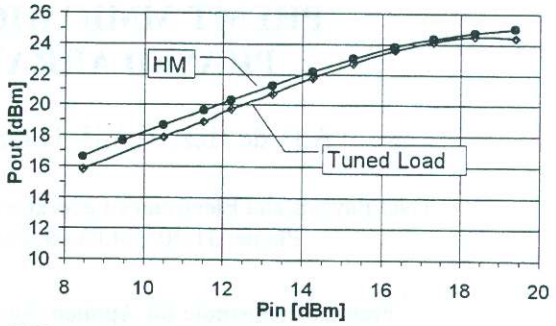

Fig.5: Measured output power for the tuned load (unmanipulated) design and for the HM approach

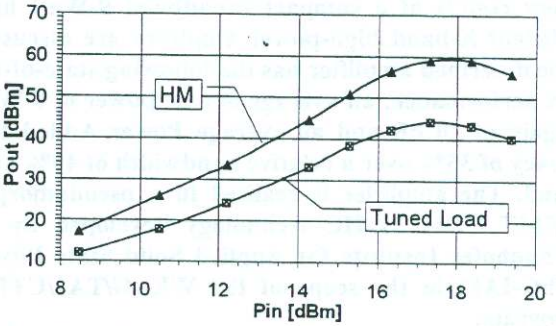

Fig.6: Measured power-added efficiency for the tuned load (unmanipulated) design and for the HM approach.

V. REFERENCES

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