Change of $g_m(f)$ in LT-GaAs and LT-$Al_{0.3}Ga_{0.7}As$ MISFETs with Thermal Stress

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Abstract — **GaAs and $Al_{0.3}Ga_{0.7}As$ layers grown by MBE at low temperatures (LT) and subsequently annealed at normal growth temperature (600^{0}C) were used as insulators in the gate structure of GaAs MISFETs. We observed improvement in the transconductance (g_m) frequency dispersion characteristics of MISFET devices when compared to that of MESFETs. The high resistivity of *in-situ* annealed LT-grown insulator layers are due to arsenic precipitates and deep centres. Under long-term operation these defects might migrate towards the interface and deteriorate the g_m frequency dispersion characteristics. To validate these MISFET devices for long-term operation, g_m frequency dispersion studies were carried out before and after thermal stressing.**

I. INTRODUCTION

The maximum output power that can be obtained from GaAs MESFETs is limited by i) low gate-drain breakdown voltage[1] and ii) onset of gate conduction[2]. These factors can be improved by introducing an insulator beneath the gate and using the same material for surface passivation for the exposed areas of gate-drain and gate-source spacings. Native oxides and heteromorphic insulators did not become popular because of one or more of the following reasons[2]: 1) Low resistivity, 2) Low breakdown field strength, and 3) High density of interface states. GaAs and $Al_xGa_{1-x}As$ layers grown at 200^{0}C-300^{0}C and subsequently *in situ* annealed at 600^{0}C, have proven to be valuable in both electronic and optoelectronic applications owing to their high resistivity and high breakdown field. MISFETs with LT-GaAs insulators[3] have shown power handling capability of 1.57W/mm at 1.1GHz which has exceeded the highest reported value of 1.4W/mm[4] for GaAs based MESFETs. The insulating nature of the annealed LT grown layers is due to the arsenic precipitates and deep centres. These defects have been successfully confined to the LT layers by sandwiching the LT layers between thin AlAs outdiffusion barriers[5]. Chen et al[6] reported improvement in the frequency dispersions of the transconductance and output resistance of MESFETs, when LT-GaAs was used as the surface passivation layer. When the LT-layers are used as gate insulators, apart from playing the role of reducing the on-set of gate conduction, it also passivates the gate-drain and the gate-source spacings. This should result in better transconductance frequency dispersion characteristics when compared to MESFETs, apart from improving the gate-drain breakdown voltage and power performance. Since the insulating nature of LT-layers is due to arsenic precipitates and deep centres, they might post a threat to the device functionality under long term operation. On these lines, studies of the change of transconductance frequency dispersion before and after thermal stressing were carried out.

II. EXPERIMENT

The LT-GaAs or LT-$Al_{0.3}Ga_{0.7}As$ MISFET structures shown in Fig. 1b were grown on semi-insulating GaAs substrates with a Riber 32P MBE system. The LT-layers, which can be either LT-GaAs or LT-$Al_{0.3}Ga_{0.7}As$ were sandwiched between two 100Å thick AlAs barrier layers to prevent the outdiffusion of excess arsenic incorporated during the LT-layer growth. The top 100Å AlAs layer was capped with a 100Å thick undoped GaAs layer. The active layer consisted of a 1800Å thick GaAs layer doped to 2.2×10^{17} cm^{-3} with Si. All the LT-layers in this study were grown at 280^{0}C and the conventional layers were grown at 600^{0}C. A 10min *in-situ* annealing at 600^{0}C of the LT-layers was carried out under arsenic overpressure. Devices with nominal gate lengths of 2μm were fabricated on all wafers using conventional mesa isolation technique. Ohmic contacts for source and drain of the MISFETs were formed by depositing AuGe/Ni/Au on to the n-GaAs active layer after selectively etching the gate insulator and were subsequently annealed at 425^{0}C for 20s in a rapid thermal processing (RTP) furnace under nitrogen flow. The gates for the MISFET were formed by depositing Ti-Au metal with a source drain separation of 6μm. MESFETs with same dimensions have been fabricated for comparison purpose. For MESFETs, after achieving the desired drain current by recess etching, Ti/Au was deposited. LT-layers with thickness of 1000Å and 250Å were considered for our studies. The Detailed processing steps of MISFETs are presented by Rao et al. [2].

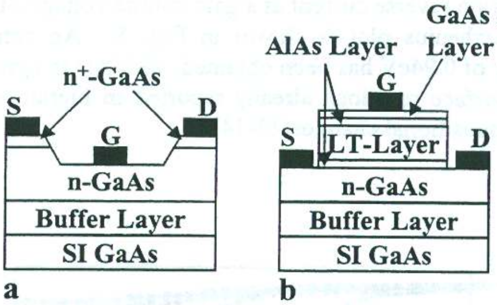

Fig. 1.. Cross-sections of a) MESFET and b) MISFET devices.

Room temperature electrical measurements were carried out using a HP-4156A precision semiconductor parameter analyzer. The parameters that were determined were near-zero-gate-bias transconductance g_m, saturated source drain current at zero gate-bias I_{DSS}, gate-to-source voltage , V_{GS} (measured at V_{DS}=3V and I_{DS}=1.5mA, i.e., 10 mA per 1mm of gate width) and gate breakdown voltage, V_{BD} measured at a gate current of 1mA/mm with both source and drain at ground. High temperature aging of these devices was carried out at 210^{0}C for durations up to 1000h after mounting the devices in TO-5 cans. Electrical measurements were carried out at regular intervals to determine the thermal stability of the aforementioned device parameters. Transconductance frequency dispersion studies were carried out using the similar setup described by Golio et al.[7].

III. RESULTS AND DISCUSSION

The devices that were subjected to reliability studies were screened using drain voltage with gate at pinch-off voltage as criteria. Only devices passing a screening drain voltage of 10V for MESFETs and 20V for MISFETs with gate at pinch-off were accepted for the accelerated aging studies. All these devices were subjected to thermal stress at 210^{0}C and the results are shown in Fig. 2.

From the results it can be clearly seen that in MISFETs the degradation in g_m and I_{DSS} is less when compared to that of MESFETs. The degradation in V_{GS} and V_{BD} for 1000Å thick LT-GaAs MISFETs is relatively higher than that for MESFETs. One plausible reason for this degradation could be due to defect migration towards the insulator and active layer interface thus contributing to the higher source-drain leakage current. These defects might generate anomalous and undesirable characteristics in these devices affecting critical electrical characteristics such as the transconductance frequency dispersion, $g_m(f)$. A decrease of g_m with increasing frequency can be observed especially when the device is operated at low drain voltage in the ohmic region of the current-voltage characteristics[8-9], if states are present at the active layer surface. The g_m dispersion with frequency occurs when the occupancy of the defects at the interface is not able to follow the signal, i.e., when the characteristic frequency of the defects is lower that of the applied signal.

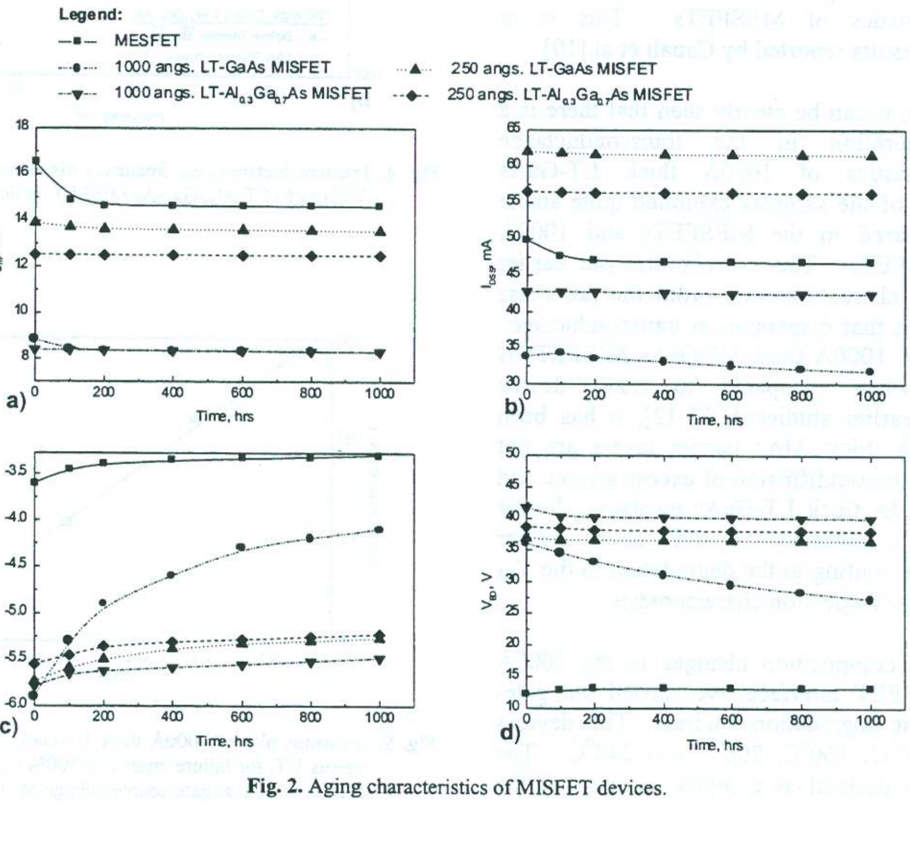

Fig. 2. Aging characteristics of MISFET devices.

To confirm defect migration, transconductance frequency dispersion studies were carried out before stressing and after stressing for 1000h at 210^0C. For all these experiments, the transconductance was measured from 20Hz to 100kHz for a 200mV signal. The MESFET and MISFETs were biased below saturation with a drain voltage of 0.5V and gate voltage of -1.0V. The resultant transconductance frequency dispersion characteristics of the MESFETs are shown in Fig. 3 and those of LT-GaAs and LT-$Al_{0.3}Ga_{0.7}As$ MISFETs in Fig. 4a and Fig. 4b respectively.

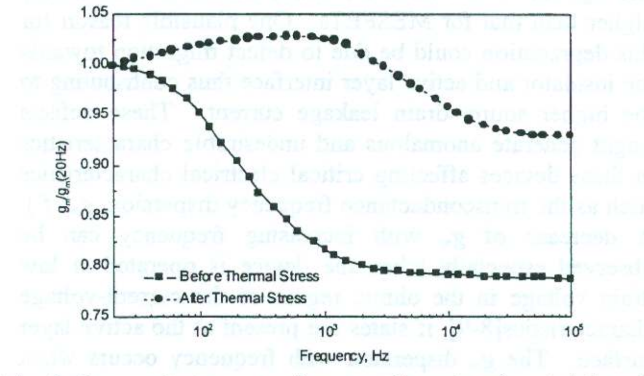

Fig. 3. Transconductance, g_m, frequency dispersion characteristics of MESFET.

We observed an improvement in the frequency dispersion characteristics of MESFETs. This is in agreement with the results reported by Canali et al.[10].

From the results, it can be clearly seen that there is a considerable deterioration in the transconductance dispersion characteristics of 1000Å thick LT-GaAs MISFETs. The rest of the samples exhibited quite stable characteristics compared to the MESFETs and 1000Å thick LT-GaAs MISFETs. This corroborates our earlier findings from aging characteristics. From the pre-stress results, it can be seen that dispersion in transconductance with frequency in the 1000Å thick LT-GaAs MISFETs is relatively higher when compared to other device structures. In our earlier studies[2, 11-12], it has been confirmed that 100Å thick AlAs barrier layers are not sufficient to prevent the outdiffusion of excess arsenic and deep defects for 1000Å thick LT-GaAs insulator. Under thermal stress, this interface would have further deteriorated thus contributing to the degradation in the V_{GS} and V_{BD} and frequency dispersion characteristics.

To confirm the composition changes in the 1000Å thick LT-GaAs MISFET interface, we carried out gate-drain reverse current degradation studies. The devices were stressed at 120^0C, 160^0C, 200^0C and 240^0C. The failure criterion was defined as a 500% increase of the gate-drain reverse current at a gate-source voltage of -12V. The Arrhenius plot is shown in Fig. 5. An activation energy of 0.94eV has been obtained, which is in agreement with surface reactions already reported in literature, such as compositional changes[13-14].

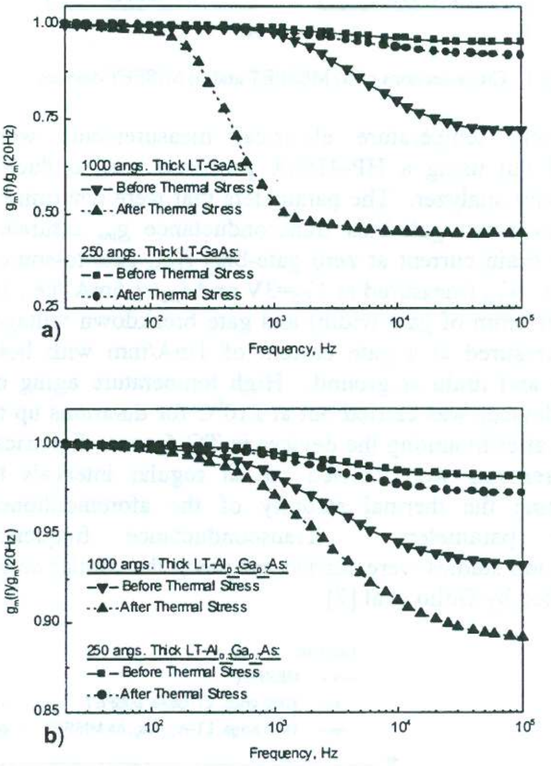

Fig. 4. Transconductance, g_m, frequency dispersion characteristics of a) LT-GaAs b) LT-$Al_{0.3}Ga_{0.7}As$ MISFET devices.

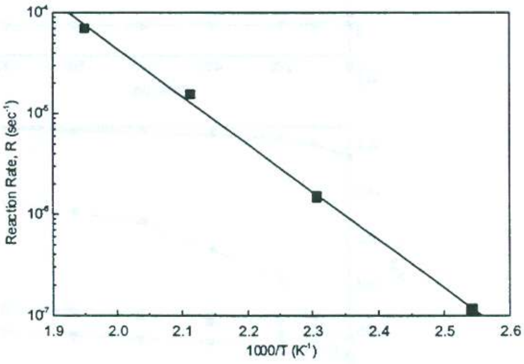

Fig. 5. Arrhenius plot of 1000Å thick LT-GaAs MISFET, reaction rate versus 1/T, for failure criteria of 500% increase of the gate-drain reverse current at gate-source voltage of -12V.

IV. CONCLUSIONS

All the LT-$Al_{0.3}Ga_{0.7}As$ samples and 250Å thick LT-GaAs samples exhibited stable characteristics for thermal stressing at 210^{0}C up to 1000 hrs. 1000Å thick LT-GaAs samples exhibited considerable degradation with stressing. Transconductance frequency dispersion studies before and after thermal stressing confirmed the compositional changes at the interface in thicker LT-GaAs MISFET structures.

V. ACKNOWLEDGEMENTS

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VI. REFERENCES

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