SiGe Bipolar ICs With Data Rates From 40 to 60 Gb/s For Future Fiber-Optic Systems

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Abstract: *This paper gives a review on a chip-set of very-high-speed ICs for fiber-optic TDM systems realized in a SiGe bipolar laboratory technology. With the uncritical circuits like time-division multiplexer and demultiplexer record data rates of 60 Gb/s were achieved. But even the speed-critical modulator driver and transimpedance amplifier proved to be suited for operation at 40 Gb/s, if an adequate configuration of the TDM system is chosen. It should be noted, that all the experimental results presented, are measured on* mounted *chips, using conventional wire bonding.*

1. Introduction

Today, commercial time-division multiplexing (TDM) systems for long-haul optical-fiber links are running at 2.5 and 10 Gb/s, respectively. To meet the increasing demand on transmission capacity for future TDM systems 40 Gb/s are under discussion. Even with the worldwide best laboratory technologies the developement of ICs for such a high data rate remains a challenging task. Further applications for ultra-high-speed TDM systems will be local area networks as well as interconnections in high-speed switching networks and multiprocessor computers.

For Si-based technologies we recently demonstrated, that all ICs required in a TDM link running at 40 Gb/s can be realized in an advanced SiGe technology [1]. This paper briefly summarizes the results and considerations for the ICs suitable for operation at maximum data rates from 40 to 60 Gb/s .

In order to achieve 40 Gb/s even with the speed-critical circuits, a configuration of the TDM system as shown in Fig. 1 is used. It allows relaxed specifications for the ICs compared to conventional 10 and 20 Gb/s systems and is similar to the one applied in a 40 Gb/s TDM system of the German R&D program Photonik II [2, 3].

In the transmitter, the conventional MUX, described in Sec. 3.1, is replaced by a power version of this circuit ("power MUX") described in Sec. 3.2. The power MUX stands out for steeper pulse edges and smaller time jitter compared to the conventional modulator driver which operates at the edge of its speed performance (Sec. 3.3). However, both driver concepts require a symmetrical configuration of the electroabsorption modulator (EAM) in order to halve their output swing. In the receiver, a gain-controlled optical amplifier (OA) is used in front of the photodiode (PD) in order to relax the specifications on gain, dynamic range and input sensitivity of the succeeding transimpedance amplifier (TIA), presented in Sec. 3.4. The decision function is performed by a 1:2 DEMUX (clock frequency 20 GHz) described in Sec. 3.5, which stands out for a high operating speed at excellent retiming capability, and a high input sensitivity compared to a single MS-D-FF (clock frequency 40 GHz). An experimental verification, applying the DEMUX for the decision function in a 40 Gb/s clock and data recovery multi-chip module is shown in [4].

2. SiGe Bipolar Technology And Mounting Technique

All circuits were realized in a SiGe laboratory technology of Infineon (formerly Siemens) [5]. It is a self-aligned double-polysilicon technology with 0.5 μm lithography (resulting in an effective emitter stripe width of $b_E = 0.3$ μm) and three metallization layers. A gradient of the Ge concentration in the epitaxial base causes an accelerating drift field, which reduces the transit time τ_f and thus increases f_T (=72 GHz) and f_{max} (=74 GHz). The speed potential is further increased by the high admissible collector current density of $j_{CK} \approx 2$ mA/μm^2 (at V_{CE}=1V). Typical parameters for a transistor with 10 μm emitter length are junction capacitances of C_{EB}=28 fF, C_{CB}=19 fF, C_{CS}=20 fF, and a base resistance of $r_B = 35$ Ω.

Besides the TIA and the power MUX for which Al_2O_3 ceramic substrates and an industrial measurement socket with low thermal resistance (only for power MUX) were used, all the ICs were mounted in a simple and inexpensive way, which proved to be suited for data rates up to 60 Gb/s. Fig. 2 shows schematically the chip and the surrounding part of the measurement socket, which consists of a 254 μm thick teflon substrate (PTFE) with low permittivity ($\varepsilon_r = 2.2$) soldered on a brass block [6]. The chip is glued into a recess in this socket

and then conventionally ultrasonic bonded. By this measure, the chip surface is about at the same level as the microstrip line, so that the bond-wire lengths and thus the bond inductances are reduced (about 0.3 nH for a single wire). Due to differential operation, the effective (odd-mode) bond inductance is further reduced by keeping the bond wires in parallel and close together.
A photograph of the complete measurement socket for the 60 Gb/s MUX described in more detail in [7], is shown in Fig. 3. At the data inputs (30 Gb/s) and the clock input (30 GHz) K-connectors are used. To achieve a low reflection coefficient at the output (60 Gb/s), a semi-rigid cable, whose diameter fits the substrate thickness, was directly connected to the measurement socket by means of a simple fixture. Similarly good results were obtained with K-connectors in a slightly modified assembly compared to the manufacturer's instructions.

3. Experimental Results Of The High-Speed ICs

3.1. 60 Gb/s MUX [7]

The MUX consists mainly of the MUX-core and two emitter-follower pairs as data input buffers. A separate output buffer is not applied, in order to obtain maximum operating speed. The MUX-core was designed to switch 10 mA, resulting in a differential output voltage swing of 0.5 $V_{p\text{-}p}$ at 50-Ω on-chip matching and 50 Ω external load. Design aspects are given in [8], and, more generalized, in [6]. The power consumption is 300 mW at a single supply voltage of -5 V. For a chip photograph of the MUX see [8].
Fig. 5 shows the differential output eye diagram of the MUX chip mounted in the socket in Fig. 3 at an output data rate of 60 Gb/s. The rise and fall times (20 to 80%) of the pulse edges are about 7 ps, including the degradation caused by the limited bandwidth of the measurement setup and the sampling scope (HP 54124). As shown in [7], also the time jitter is considerably degraded by the measurement equipment. However, the "eyes" are sufficiently open and the clock phase margin is still 130°, demonstrating the retiming capability even at this data rate. Although this MUX is not required in the proposed transmitter concept in Fig. 1, it is a useful device in very-high-speed applications, e.g. as the final MUX in the output stage of our bit-pattern generator [7], which is applied to the measurements of all the ICs presented in this paper.

3.2. Power MUX As A Modulator Driver [9]

In order to benefit from the inherent high speed capability of the MUX, we designed a power version of the 60 Gb/s MUX to drive directly the EAM. The simplified block diagram of the power MUX is shown in Fig. 4a. Completely differential operation is applied. Besides the much higher switched output current (up to 50 mA), the main differences compared to the 60 Gb/s MUX are as follows. At the (50-Ω) data inputs, more powerful buffer stages are used, which each consist of a current switch with two EF pairs at its input and three at its output. Using only two or three EF pairs as a buffer would result in large input transistors and thus in a high input capacitance (in parallel to the 50-Ω on-chip resistors), which would severely degrade transmission line matching. Moreover, comparatively large signal amplitudes would be required at the data inputs. At the output of the MUX-core a (differential) grounded-base stage (GBS) is used, in order to mitigate the transistor breakdown problems and to increase the operating speed. At the differential output, in series to the load resistors $R_Q = 25\ \Omega$ a network is realized on the chip, which biases the EAM and, in addition, partly compensates for its low-pass characteristic by peaking [10]. The EAM bias voltage V_{Bias} can be varied between 0 V and -2 V via an external potentiometer, at a nominal value of -1 V. To halve the voltage swing at each of the complementary outputs, a symmetrical EAM configuration is used, which can be driven by a differential voltage swing of 2 $V_{p\text{-}p}$ (2×1 $V_{p\text{-}p}$). A more detailed description of the circuit and its output stage is given in [9] and [10], respectively, together with design aspects.
For the measurements the chip was mounted on a special measurement socket with low thermal resistance. Al_2O_3 ceramic substrate and K-connectors were applied. The total power consumption at the two supply-voltages of +4 V and -6.5 V is 2 W.
As discussed in detail in [10], the signal across the EAM quantum wells agrees well with the output signal measured with an a.c. coupled 50 GHz sampling scope (HP 54124). For this, the on-chip resistances R_Q must be increased from 25 Ω to 50 Ω (by scratching on-chip interconnections). As a consequence, the correct operation of the driver circuit can be verified by pure electrical measurements.
The power MUX was driven by the same measurement setup as used for the 60 Gb/s MUX in [7]. The *differential* voltage swing at the data inputs was chosen as low as 300 m$V_{p\text{-}p}$ for all measurements, in order to demonstrate the comparatively high gain of the circuit. The voltage swing of the *differential* sinusoidal clock signal is 1 $V_{p\text{-}p}$

at 40 Gb/s and 1.5 $V_{p\text{-}p}$ at 50 Gb/s, respectively. Fig. 4b (top) shows the measured output eye diagram at the nominal data rate of 40 Gb/s with a differential voltage swing of 2.5 $V_{p\text{-}p}$. Well opened "eyes" with small time jitter can be observed. The clock phase margin measured at this data rate is 135°, confirming the retiming capability of the circuit. Even at 50 Gb/s, sufficiently clear output eye diagrams are obtained at the nominal swing of 2 $V_{p\text{-}p}$, as shown in Fig. 4b (bottom), demonstrating the high speed potential of the power MUX. Both eye diagrams in Fig. 4b are given for the nominal EAM bias voltage V_{Bias}= -1 V, but no degradation of signal performance was observed within the adjustable bias range of 0 to -2 V.

3.3. Modulator Driver [10]

In addition to the power MUX, a conventional EAM driver was designed and fabricated in the same technology. Its output stage, consisting of a grounded-base stage as well as an EAM biasing and peaking network, is the same as in the case of the power MUX (cf. Fig. 4a) [10]. The measurement result in Fig. 6 still shows a clear eye diagram at 40 Gb/s and 2.5 $V_{p\text{-}p}$ differential output swing. However, the measurements confirm that a data rate of 40 Gb/s is near to the speed limit of this circuit - in contrast to the power MUX (cf. Fig. 4b). Therefore, the power MUX, which additionally stands out for its retiming capability, is confirmed to be the superior solution for this application.

3.4. Transimpedance Amplifier [11]

To reduce costs and avoid critical interfaces, the amplifier was not separated into a preamplifier and a main amplifier; instead, the total amplifier was realized on a single chip. Fig. 7a shows the block diagram of the transimpedance amplifier (TIA) with three basic amplifier cells. For all cells a fully differential configuration was chosen. Besides other advantages, this measure helps to reduce performance degradation caused by substrate coupling as well as by on-chip wiring and mounting parasitics. As shown in the simplified circuit diagram in Fig. 7b, each cell consists of a transimpedance (TIS) and a transadmittance stage (TAS) (with a grounded-base stage (GBS) at the output to mitigate potential transistor breakdown problems) decoupled by three emitter-follower pairs (EF). At the output of the third cell (output stage), which must drive a (differential) 50-Ω transmission line, on-chip output resistors (60 Ω) are used to reduce double reflections.

At the high gain required, 40 Gb/s can hardly be reliably achieved with completely linear operation. Therefore, only the first amplifier cell operates in the linear and the others in the limiting mode. As another advantage of limiting operation, the constant output voltage swing is obtained without needing automatic gain control.

In order to cancel the offset current which depends on the signal amplitude of the input current i_I, automatic offset control, using a d.c. amplifier and a low-pass (LP) filter, is applied. An additional contribution to the input offset current can be adjusted (not shown in Fig.7a) to optimize the switching threshold, for minimizing the bit error rate of the receiver (especially if optical amplifiers are applied).

The amplifier chip (size: 0.9 mm × 1.4 mm) was mounted on a measuring socket applying Al_2O_3 ceramic substrate and K-connectors. In addition, for the pure electrical measurements the simplified PD model shown in Fig. 7a (bottom) was realized on the substrate of the measurement socket [11]. It exhibits a total PD capacitance of 65 fF and a 50-Ω line termination for the driving bit-pattern generator.

Fig. 7c shows the measured clear output eye diagram of the differential output voltage v_Q at 40 Gb/s, for the lower limit of the input current swing, $\Delta I_I = 0.3$ $mA_{p\text{-}p}$. Even better signal quality (at the same output voltage swing of $\Delta V_Q = 0.6\,V_{p\text{-}p}$) was observed at the upper specified limit of input current swing, $\Delta I_I = 0.6\,mA_{p\text{-}p}$ (not shown in Fig. 7). Thus the maximum large-signal transimpedance in the limiting mode is $Z_{TI} = \Delta V_Q/\Delta I_I = 2\,k\Omega$ (while the small-signal transimpedance proved to be 10 kΩ). The total power consumption of the TIA is 800 mW at a single supply voltage of -6.5 V.

3.5. 60 Gb/s DEMUX [12]

Fig. 8a shows the block diagram of the 1:2 DEMUX which consists of the DEMUX-core with two MS-D-FFs operating in parallel, data and clock input stages, and two output buffers. Circuit diagrams of these building blocks have already been presented and discussed e.g. in [13] and [14] and shall, therefore, not be recapitulated here. The total power consumption of the DEMUX is 1.2 W at a single supply voltage of -5 V, including 0.6 W of the oversized high-speed output buffers taken from a modular concept [13, 12].

The chip was mounted as described in Sec. 2 and driven by a bit-pattern generator with the 60 Gb/s MUX as the last stage. As in the case of the MUX, the clock frequency is 30 GHz. The measured eye diagram of the driving bit-pattern in Fig. 8b (top) is intentionally degraded in order to demonstrate the excellent retiming capability

of the DEMUX even at 60 Gb/s. The output eye diagram in Fig. 8b (bottom), measured for an on-chip output resistance of 100 Ω, is well opened and shows only small time jitter at a differential voltage swing of 640 $mV_{p\text{-}p}$. The CPM for this measurement is estimated to be about 180° at a swing of the *differential* sinusoidal clock signal of 1.5 $V_{p\text{-}p}$.
Due to the intended application of the IC as a DEMUX with additional decision function in the receiver of a 40 Gb/s system, the CPM versus differential input data swing was measured at this data rate. The results in Fig. 8c demonstrate the high sensitivity and excellent retiming capability of this circuit. This is of special interest since, to the best of the authors' knowledge, single MS-D-FFs with such a high CPM and sensitivity at 40 Gb/s (i.e. at 40 GHz clock frequency) have not yet been reported. Therefore, for the decision function in the receiver of 40 Gb/s TDM systems the DEMUX should be preferred to the speed-critical MS-D-FF.

4. Conclusions

A chip-set of very-high-speed ICs for future fiber-optic systems realized in a SiGe technology has been presented. It has been shown by measurements of the *mounted* chips, that even the speed-critical ICs are suitable for operation in future 40 Gb/s TDM systems. However, for reliable operation, an adequate configuration of the TDM system has to be chosen, which allows relaxed specifications for these ICs.

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References

1. H.-M. Rein, "Si and SiGe bipolar ICs for 10 to 40 Gb/s optical-fiber links", (1999), *High-Speed Circuits for Lightwave Communications* edited by K.-C. Wang, in "Selected Topics in Electronics and Systems", edited by P.K. Tien, World Scientific Publishing, Singapore, Vol. 13, pp. 35-71.
2. E. Gottwald, A. Felder, H.-M. Rein, M. Möller, M. Wurzer, B. Stegmüller, M. Plihal, J. Bauer, F. Auracher, W. Zirwas, U. Gaubatz, A. Ebberg, K. Drögemüller, C. Weiske, G. Fischer, P. Krummrich, W. Bogner and U. Fischer, "Towards a 40 Gbit/s electrical time division multiplexed optical transmission system", (1996), *Proc. ICCT '96*, Beijing, China, pp. 60-63.
3. H.-M. Rein, E. Gottwald and T.F. Meister, "Si-bipolar - A potential candidate for high-speed electronics in 20 and 40 Gb/s TDM systems?", (1997), in *Proc. OSA Spring Topical Meetings '97:Ultrafast Electronics and Optoelectronics*, Incline Village, Nevada, invited paper UTUA1-1, pp. 118-120, and in OSA Trends in Optics and Photonics Series 13: Ultrafast Electronics and Optoelectronics, Optical Society of America, pp. 124-128.
4. W. Bogner, "40 Gb/s decision, demultiplexer and clock recovery circuit for ultra high speed optical transmission systems", Technical Report, Siemens AG, Munich, published on the internet: http://www.siemens.de/ic/networks/products/optitran/worldrec/index.htm
5. T.F. Meister, H. Schäfer, M. Franosch, W. Molzer, K. Aufinger, U. Scheeler, C. Walz, M. Stolz, S. Boguth and I. Böck, "SiGe base bipolar technology with 74 GHz fmax and 11 ps gate delay", (1995), *Tech. Dig. IEDM '95*, Washington, pp. 739-742.
6. H.-M. Rein and M. Möller, "Design considerations for very-high-speed Si-bipolar IC´s operating up to 50 Gb/s", (1996), *IEEE J. Solid-State Circuits*, Vol. 31, pp. 1076-1090.
7. M. Möller, H.-M. Rein, A. Felder and T.F. Meister, "60 Gbit/s time-division multiplexer in SiGe-bipolar technology with special regard to mounting and measurement technique", (1997), *Electron. Lett.*, Vol. 33, pp. 679-680.
8. M. Möller, H.-M. Rein, A. Felder, J. Popp and J. Böck, "50 Gbit/s time-division multiplexer in Si-bipolar technology", (1995), *Electron. Lett.*, Vol. 31, pp. 1431-1433.
9. M. Möller, T.F. Meister, R. Schmid, J. Rupeter, M. Rest, A. Schöpflin and H.-M. Rein, "SiGe retiming power MUX for driving an EAM up to 50 Gbit/s", (1998), *Electron. Lett.*, Vol. 34, pp. 1782-1784.
10. R. Schmid, T.F. Meister, M. Rest and H.-M. Rein, "40 Gbit/s EAM driver IC in SiGe bipolar technology", (1998), *Electron. Lett.*, Vol. 34, pp. 1085-1097.
11. J. Müllrich, T.F. Meister, M. Rest, W. Bogner, A. Schöpflin and H.-M. Rein, "40 Gbit/s transimpedance amplifier in SiGe bipolar technology for the receiver in optical-fibre links", (1998), *Electron. Lett.*, Vol. 34, pp. 452-453.
12. A. Felder, M. Möller, M. Wurzer, M. Rest, T.F. Meister and H.-M. Rein, "60 Gbit/s regenerating demultiplexer in SiGe bipolar technology", (1997), *Electron. Lett.*, Vol. 33, pp. 1984-1985.
13. J. Hauenschild, A. Felder, M. Kerber, H.-M. Rein and L. Schmidt, "A 22 Gb/s decision circuit and a 32 Gb/s regenerating demultiplexer IC fabricated in silicon bipolar technology", (1992), *Proc. IEEE BCTM* '92, Minneapolis, pp. 151-154.
14. A. Felder, M. Möller, J. Popp, J. Böck and H.-M. Rein, "46 Gb/s DEMUX, 50 Gb/s MUX, and 30 GHz static frequency divider in silicon bipolar technology", (1995), *IEEE J. Solid-State Circuits*, Vol. 31, pp. 481-486.

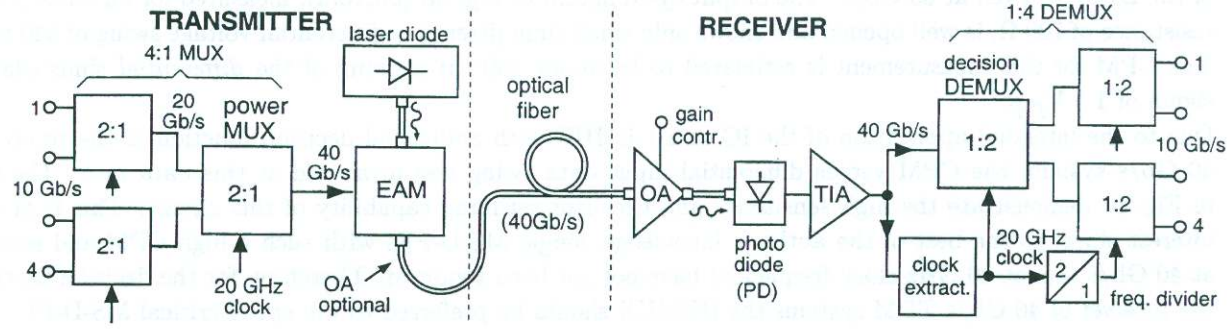

Fig. 1. Scheme of a 40 Gb/s optical-fiber TDM link with relaxed specifications for the speed-critical circuits. For simplification, the loop for the automatic gain control of the optical amplifier (OA) as well as additional connections between decision DEMUX output and clock extraction circuitry [4] are not shown.

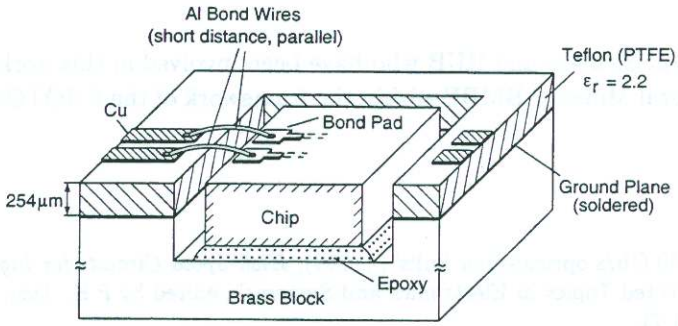

Fig. 2. Scheme of the simple mounting technique used for most of the high-speed ICs. The bond wires are shown for a differential signal line.

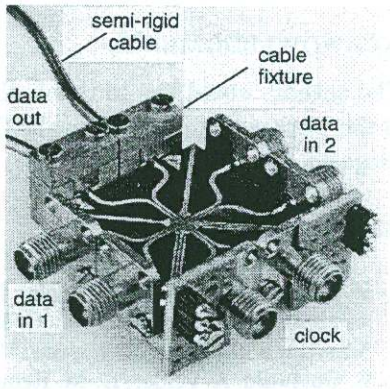

Fig. 3. Measurement socket of the 60 Gb/s MUX. Size of substrate is about 3 cm × 3 cm.

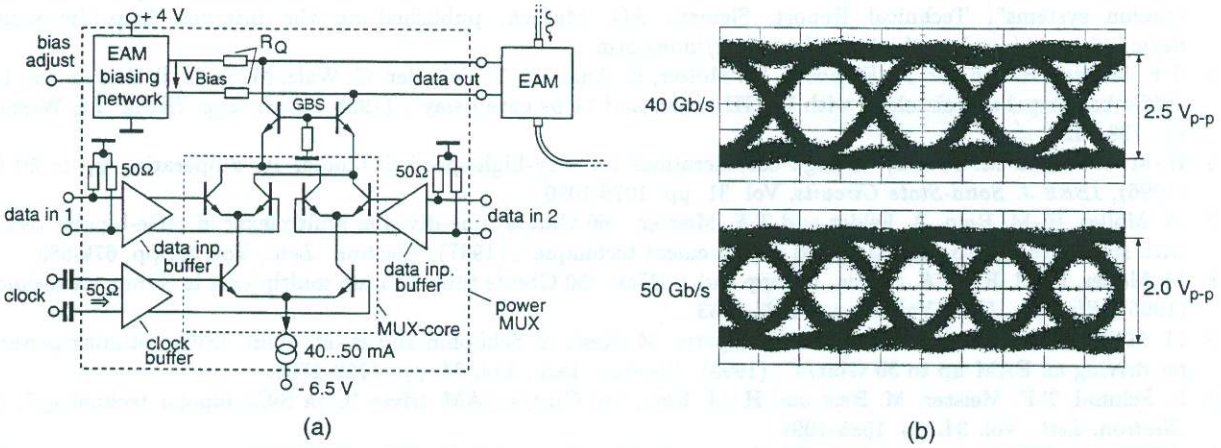

Fig. 4. Power MUX for driving the EAM in a 40 Gb/s link. (a) Simplified block diagram. (b) Output eye diagrams at 40 Gb/s (top) and 50 Gb/s (bottom). Time scale: 10 ps/div.

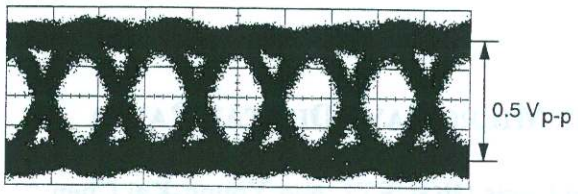

Fig. 5. Output eye diagram of the MUX at 60 Gb/s output data rate(10 ps/div.).

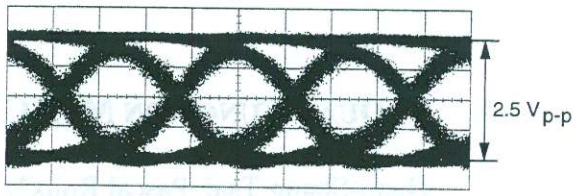

Fig. 6. Output eye diagram of a conventional EAM driver at 40 Gb/s (10 ps/div.) for comparison with the power MUX results in Fig. 4b.

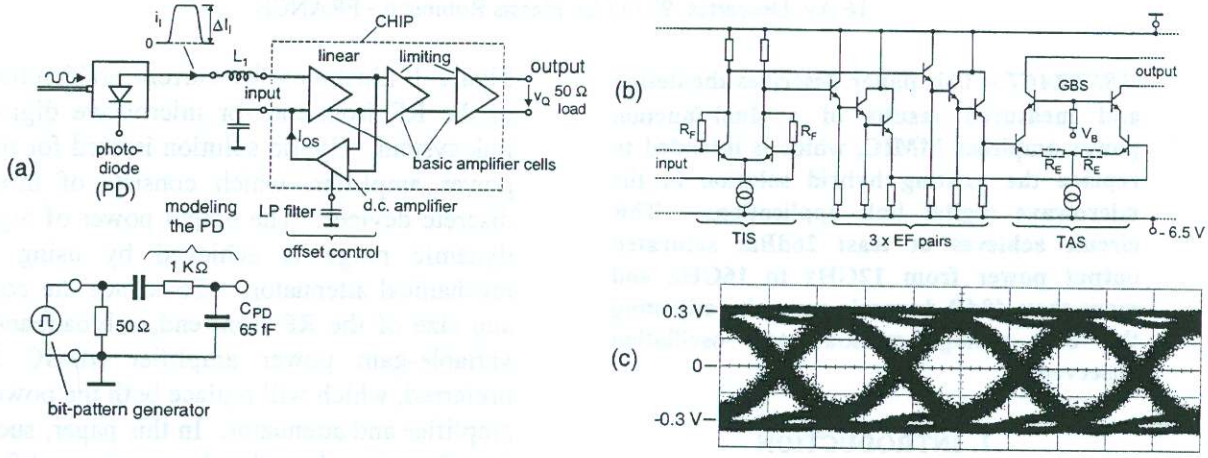

Fig. 7. Limiting transimpedance amplifier (TIA) for a 40 Gb/s link. (a) Simplified block diagram of the TIA (top) and equivalent circuit of the PD used for pure electrical measurements (bottom). (b) Basic amplifier cell. For clearness, diodes for V_{CE} reduction are not shown. (c) Output eye diagram (v_Q) at 40 Gb/s (10 ps/div.), $\Delta V_Q = 0.6\ V_{p-p}$.

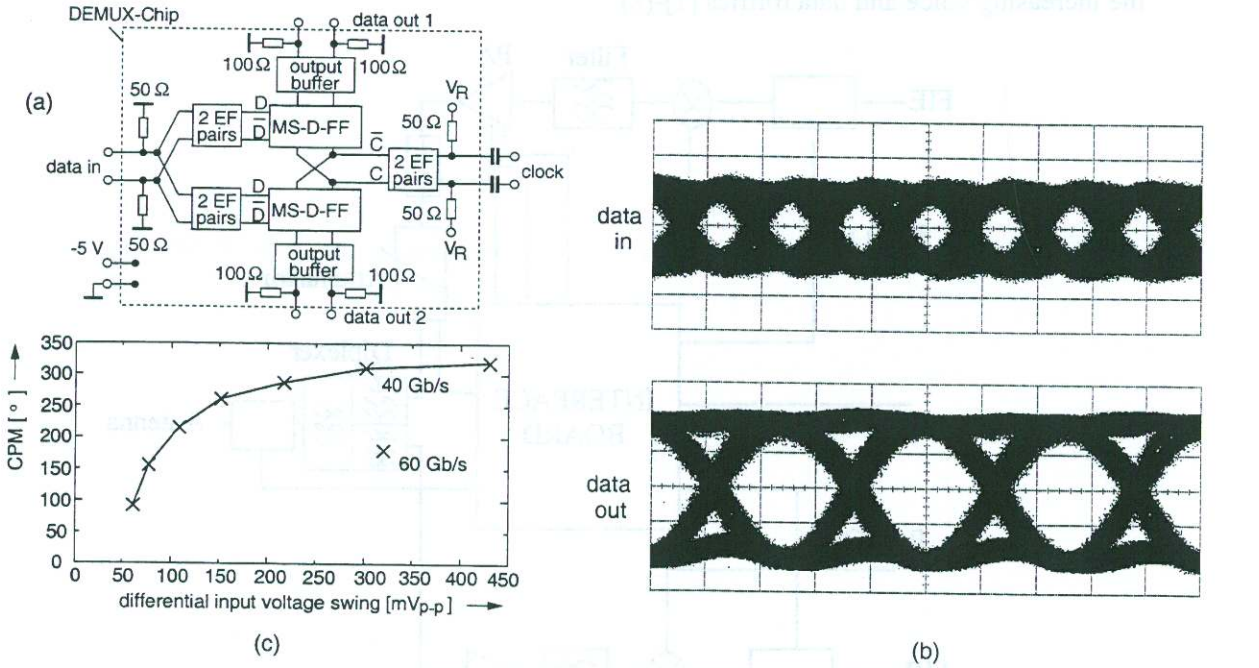

Fig. 8. Regenerating high-speed 1:2 DEMUX. (a) Block diagram. V_R is an on-chip generated bias voltage. (b) Eye diagrams at 60 Gb/s input data rate (160 mV/div., 13 ps/div.), top: intentionally deteriorated input signal (60 Gb/s), bottom: regenerated output signal (30 Gb/s), CPM $\approx 180°$. (c) Signal regeneration capability at 40 Gb/s input data rate: clock phase margin vs. differential data input voltage swing. For comparison, the measurement result from (a) at 60 Gb/s is inserted.