44 Gb/s InP DHBT MUX-Driver IC for External Laser Modulation

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Abstract: A 2 V pp 44 Gb/s MUX-Driver IC has been fabricated in self-aligned InP DHBT technology to drive a 50 Ω EAM. Optical eye diagrams have been measured up to 40 Gb/s with good extinction ratio of 9 dB.

I INTRODUCTION

Optical-fibre communication plays a major role in the present development of telecommunication and data transmission services. While 10 Gb/s systems are considered as mature enough to enter the commercial use, different approaches are compared for higher transmission rates. Terabit/s rates seem feasible as a combination of Time-Division Multiplexing (TDM) and Wavelength-Division Multiplexing (WDM) schemes. We are interested in the development of Electrical Time-Division Multiplexing (ETDM) systems which evolve rapidly toward and above 40 Gb/s per channel. At this bit rate, all components remain critical especially in the emission part of the transmission system. The main problem is to fabricate both a laser modulator providing sufficient extinction ratio with a limited input swing, and a modulator driver able to supply high voltage at such a high bit rate. The situation evolves rapidly with progress in both electro-absorption modulators development [1] and modulator drivers design [2-6]. In this contribution, a 44 Gb/s InP DHBT MUX-Driver IC is presented, driving a packaged 50 Ω / 30 GHz bandwidth EAM, also fabricated in InP technology. NRZ operation up to 40 Gb/s has been achieved: Optical eye diagrams up to 40 Gb/s with good extinction ratio (9 dB) have been measured.

II TECHNOLOGY

The circuits are fabricated in an InP DHBT self-aligned technology, developed at the OPTO+ laboratory. The InP DHBT technology is well suited for the driver design, with good frequency performances (Ft and Fmax of 125 GHz and 83 GHz have been measured for Vce = 1.6 V and J = 0.8 mA/μm^2), while keeping high gain (> 50) and high breakdown voltage (> 7 V). The use of a compositionally graded InGaAs base and self-alignment explains these good dynamic performances, reducing significantly both the transit time (graded base) and collector-base capacitance (collector undercutting allowed by self-alignment). Minimum emitter length and width of the transistors is 2.2 μm × 2.2 μm. A critical point for the design of the driver circuit is the optimal current density of the transistors. On one side, small transistors are required to satisfy high speed specifications, while an important current is necessary to obtain a high output swing. With the used technology, current densities up to 1 mA/μm^2 are supported without degrading the circuit reliability. The technology also provides three metallic levels, allowing optimisation of routing and layout symetrisation.

III TRANSISTORS' MODELLING

Transistors are modelled using a non-linear Gummel Poon model with corrections due to specific behaviour of III-V HBT technology and inclusion of parasitic parameters for high frequency modelling. A global extraction strategy has been established to extract the 35 intrinsic model parameters. They are extracted independently from each other, in order to avoid cross correlations. Small signal parameters are determined from the (de-embedded) S parameters at different bias conditions while the large signal ones are extracted with a non-linear extraction program.
Moreover, to perform accurate design simulations, and to reach the optimal performances allowed by the technology, accurate models for a range of various transistor sizes are required. This is particularly true for the MUX-Driver circuit, because both small and large transistor sizes are used. Unfortunately, modelling such state of the art III-V HBT remains a difficult task, and extraction is only available for only few transistor sizes.
To overcome this limitation, a tool, based on analytical expressions, measurement results and the extraction procedure mentioned above, has been developed [7], to evaluate the Spice model as a function of the transistor

geometries and technological parameters. This allows us to optimise the geometries of the transistors, according to their function in the circuit.

IV CIRCUIT DESIGN

The block diagram of the MUX-Driver is presented on fig. 1. The two input data D1 and D2 at 20 Gb/s are applied through input buffers, with internal voltage references and on-chip 50 Ω resistors to match the driving transmission lines. The clock signal is directly applied to the MUX core through Emitter Followers. The signal generated by the MUX core is then reshaped and amplified by the driver.

Fig. 2 shows the circuit schematic of the driver. It consists of two differential current switches (CS) driven by Emitter Followers (EF) for level shifting and impedance transformation. For the third stage, three EFs had to be cascaded despite the consumption penalty, because of the poor efficiency of the impedance transformation at high frequencies. They have to be carefully designed in order to avoid ringing, due to their inductive, low ohmic output, combined with their capacitive input. Peaking inductances are added in series to the load resistance in order to improve the steepness of the pulse edge of the output signals. The value of the load resistance is 100 Ω to limit the switched current while avoiding distortions due to multiple reflections. Thus, the final CS has to switch a 60 mA current to achieve a 2 V output swing on 50 Ω load.

Each branch of this pair is composed of two transistors in parallel, operating at high current densities, reducing the influence of large time constants associated to the diffusion capacitance C_D proportional to the current. The main drawback of this structure is to increase interconnection lengths, degrading circuit performances.

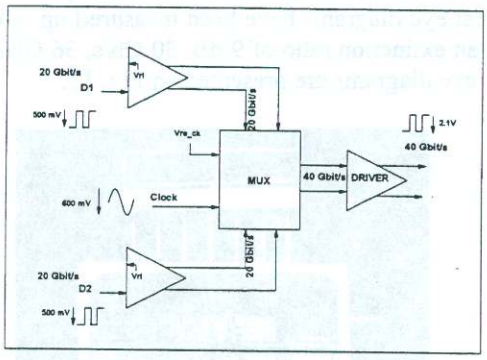

Fig. 1 : Block diagram of the MUX-Driver

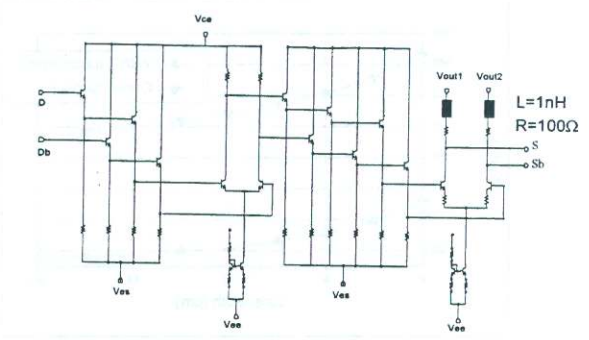

Fig. 2 : Schematic of the driver part

Layout considerations concerning VHSIC have been carefully followed [8], especially achieving symmetrical layout (microphotograph of the circuit on fig. 3) and shortening critical line lengths. But the Mux-Driver circuit remains particularly difficult to route, because of the high transient currents, the size of the transistors used and the influence of thermal constraints on design rules. Lines driven by EF stages are particularly critical, due to their low output impedance. Simulations indicate that degradations could be significantly minimised by lowering the characteristic impedance of the lines. The way to lower this impedance was to realise the internal microstrip lines with two metallic levels, one used as ground. On fig. 4 are presented some electromagnetic simulation results (HP Momentum). The characteristic impedances of a conventional microstrip line and a modified one have been calculated as a function of the line width. Values below 30 Ω have been obtained with the second structure and enable more efficient matching with the few ohms impedance of the EF driving stage.

The influence of the interconnection lines are taken into account during simulations in two steps. Firstly, the main parasitic elements are evaluated before the layout phase and included in the schematics to be simulated. Secondly, parasitic elements are automatically extracted from the layout after routing, modelled with RLC lumped elements and the circuit is then re-simulated.

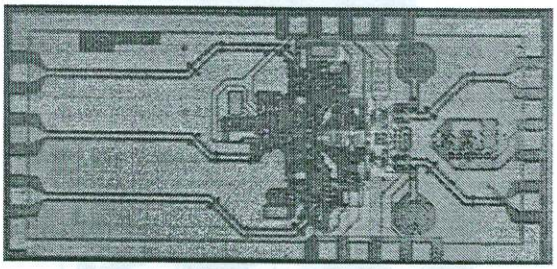

Fig. 3 : Microphotograph of the MUX-Driver

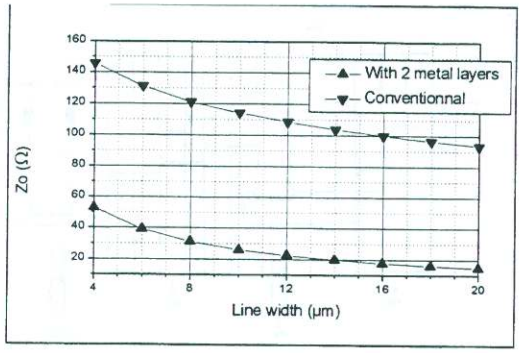

Fig 4 : Microstrip line impedance

The circuit has been mounted in a module : The chip is epoxied on a brass block and wedge bonded to a Al_2O_3 substrate plate with 50 Ω CPW lines and K connectors. A microphotograph of the final module is presented on fig. 5.

V 50 Ω CIRCUIT RESULTS

Measurements have been made on 50 Ω load (50 GHz sampling scope) using a pseudo-random bit pattern generator at 12.5 Gb/s coupled to a commercial-18 Gb/s MUX, able to operate up to 25 Gb/s. Open output eye diagrams at 40 Gb/s and at 44 Gb/s (on wafer chip) are shown on fig. 6 and 7 for a $2^{31}-1$ word length. Despite losses (due to 40 GHz picoprobes, about 80 cm K cables, and 50 GHz sampling scope), the IC provides a 2.1 Vpp output swing at 40 Gb/s, and 2 Vpp at 44 Gb/s. The 40 Gb/s output eye diagram of the packaged MUX-Driver is shown on fig. 8 (2.2 Vpp output swing). The clock phase margin measured at 40 Gb/s is 13 ps (100°) and the power consumption of the whole Selector Driver is 2.8 W (1.9 W for the driver part).

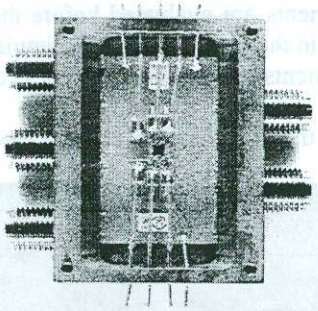

Fig. 5 : Photograph of the packaged MUX-Driver

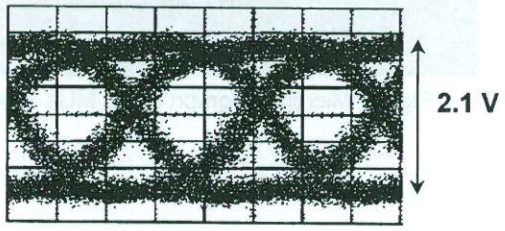

Fig. 6 : 40 Gb/s Output Eye Diagram (on wafer)

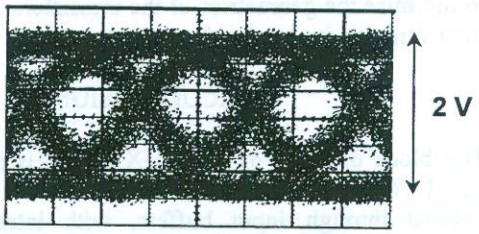

Fig. 7 : 44 Gb/s Output Eye Diagram (on wafer)

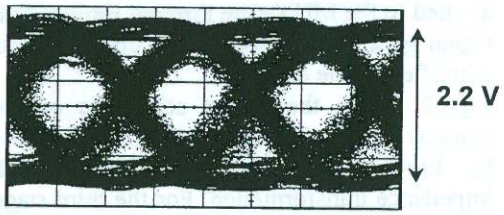

Fig. 8 : 40 Gb/s Output Eye Diagram (mounted)

VI EXTERNAL LASER MODULATION

A packaged 50 Ω Electro-absorption Modulator (presented on fig. 9) with a 30 GHz bandwidth has been fabricated [9]. The modulator provides good static extinction ratio at λ = 1548 nm, with a maximum expected static ratio of 20 dB for a 2 V driver output swing provided that the MUX-Driver IC is biased in its optimal region of operation. Unfortunately measurements constraints did not allow at this time the optimal bias to be used.

The circuit has been measured on wafer with the packaged EAM. The block diagram of the experiment is presented on fig. 10. The optical signal, modulated by the MUX-Driver / EAM combination, is amplified using an EDFA, filtered and then detected on a 50 GHz sampling scope thanks to a 32 GHz bandwidth PIN photo-detector. Optical eye diagrams have been measured up to 40 Gb/s, with an extinction ratio of 9 dB. 30 Gb/s, 36 Gb/s and 40 Gb/s eye diagrams are presented on Fig. 11.

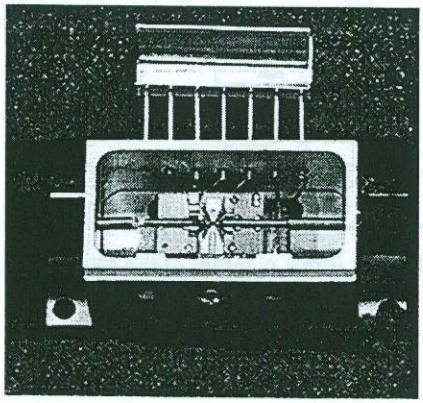

Fig. 9 : Photograph of the packaged EAM

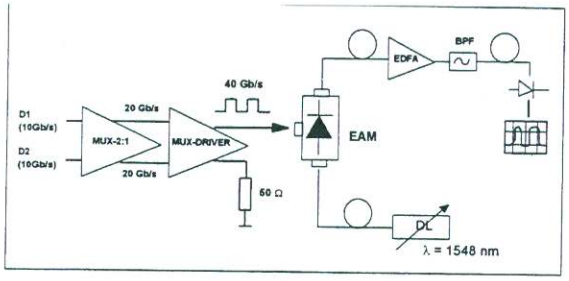

Fig 10 : Experimental set-up

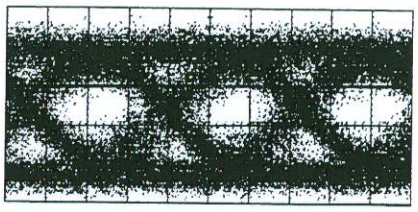

Fig. 11a : 30 Gb/s optical eye diagram

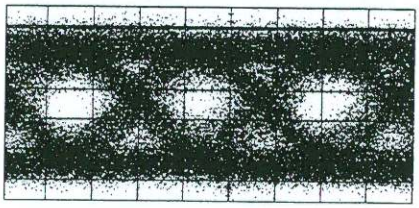

Fig. 11b : 36 Gb/s optical eye diagram

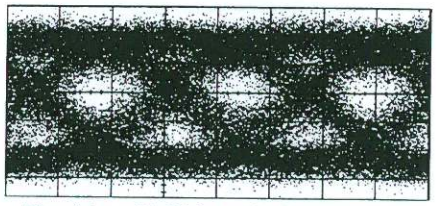

Fig. 11c : 40 Gb/s optical eye diagram

CONCLUSION

An external laser modulation for 40 Gb/s ETDM lightwave transmission system has been presented, using 44 Gb/s InP DHBT MUX-Driver and 30 GHz bandwidth InP EAM. Optical eye diagrams have been observed up to 40 Gb/s with 9 dB extinction ratio.

While using the same technology allows further promising research in the integration of both components, a MUX 2:1 has been successfully integrated with the driver IC.

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