A 2.4-V 30-dBm 61.5%-Efficiency Power PHEMT for Wireless Communications

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Abstract — **A high efficiency 2.4-V operation dual delta doped AlGaAs/ InGaAs/GaAs pseudomorphic high electron mobility transistor (PHEMT) for personal communications has been developed. The 20.16mm gate width device operating at a drain bias of 2.4 V at 1.9 GHz gives an output power of 30.0 dBm and a power added efficiency over 60%. The high efficiency at 2.4 V bias is attributed to the dual delta doped PHEMT structure which has high drain current and high electron mobility and to the shrinkage of the device layout which results in the low knee voltage and low source resistance of the device.**

I. INTRODUCTION

Advanced high performance wireless communication systems require high efficiency power transistors operating at low supply voltage. The advantages of low operation voltage include reducing power consumption of the circuits, decreasing the number of the battery cells used and the reduction of the size and weight of the system. Devices for low voltage applications have been developed in the past few years [1-4]. In this study, a low voltage 1-watt device is developed, a dual delta doped AlGaAs/InGaAs/GaAs PHEMT structure is used, this is because dual delta doped PHEMT has high current capability and high electron mobility. The device developed has a gate length of 20.16 mm with reduction in the device layout. The reduction in the device layout results in low knee voltage and low source resistance for the device.

II. DEVICE LAYOUT AND FABRICATION

The Epitaxial layer was grown by the Molecular Beam Epitaxy (MBE) technique. The structure of the dual delta doped AlGaAs/InGaAs/GaAs PHEMT is shown in Fig. 1. The active part was 85 Å InGaAs channel layer sandwiched between an upper 35Å undoped AlGaAs layer and a lower 40Å undoped GaAs layer. The two dimensional electron gas (2-DEG) was formed in the pseudomorphic InGaAs channel by electron transfer from silicon delta doping above and below the InGaAs layer. A heavily Si-doped GaAs cap was formed to provide the good ohmic contacts and reduce the source resistance. The fabricated device had a total gate width of 20.16 mm width with each finger 120 μm in length. The drain to source spacing is 4 μm and the gate length is 0.5 μm. The device covers 1665 x 350 μm^2 area, which is quite compact compared to regular power device layout. Fig. 2 is the optical photograph of a finished device. The device isolation was accomplished by wet etching using HF based solution. The ohmic metal, Au/Ge/Ni was deposited by electron-beam evaporation followed by rapid thermal annealing at 300°C for 10 seconds. Gate was formed by Ti/Pt/Au Metal. PECVD (Plasma Enhanced Chemical Vapor Deposition) silicon nitride was used for the device passivation.

III. DEVICE POWER PERFORMANCE

The device developed has a saturation current of 6A. The pinch off voltage of the device is around -1.1 V. The maximum transconductance of this device is 340 mS/mm. The breakdown voltage of this device is 12V. Fig. 3 is the I-V characteristics of the device with gate bias from –0.7 V to pinch off. The high current density and high transconductance of this device is due to the dual delta doped HEMT structure.

Power performance of this device was measured at 1.9 GHz and with a drain bias of 2.4 V. Fig. 4 shows the output power and power added efficiency as a function of the input power for the 20.16 mm wide device. The device was operated under class AB condition with a bias drain current of 400 mA. Fig. 5 is the power gain vs. input power figure for this 20.16 mm device under the above bias condition. The power characteristics were measured by a power tuning system, in which the input and output tuners with variable capacitors and inductors were used to provide the conjugate matched input and load impedances for the optimum power performance. For the 20.16 mm device, the maximum power under 2.4 V bias condition, the maximum output power is 30 dBm and the power added efficiency of this device at the maximum output power is 61.5%. The gain of this device at maximum output power is 8.47 dB. The linear gain was 11.56 dB and the output power at 1 dB compression was 28.12 dBm with a power-added efficiency of 47.5%

IV. CONCLUSIONS

A 2.4 V low voltage application power HEMT was developed. The device has a double delta doped AlGaAs/InGaAs/GaAs structure to provide high drain current density and high transconductance. The size of the layout of this device was reduced to improve the knee voltage and source resistance for low voltage applications. The device developed shows an output power of 30 dBm with a power added efficiency of 61.5% and the gain of the device at the maximum output power is 8.47 dB. The device developed should be applicable to next generation wireless communication systems.

V. ACKNOWLEDGMENT

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V. REFERENCES

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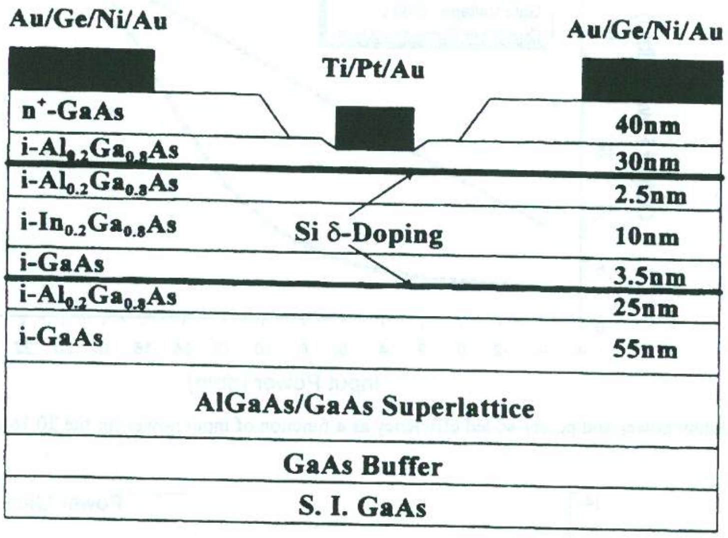

Structure of the δ-doped AlGaAs/InGaAs power HEMT.

Fig. 1 Structure of the δ-doped AlGaAs/InGaAs power HEMT.

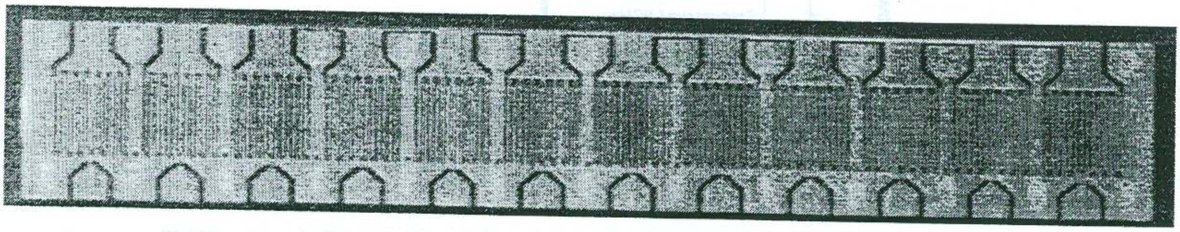

Fig. 2 The top view of the 20.16-mm-wide power PHEMT manufactured.

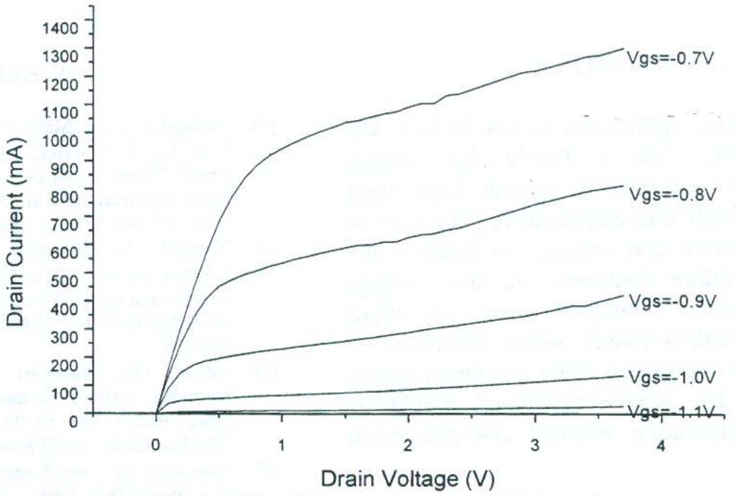

Fig. 3 The current-voltage characteristics of the 20.16-mm-wide power PHEMT with gate bias from −0.7V to pinch off.

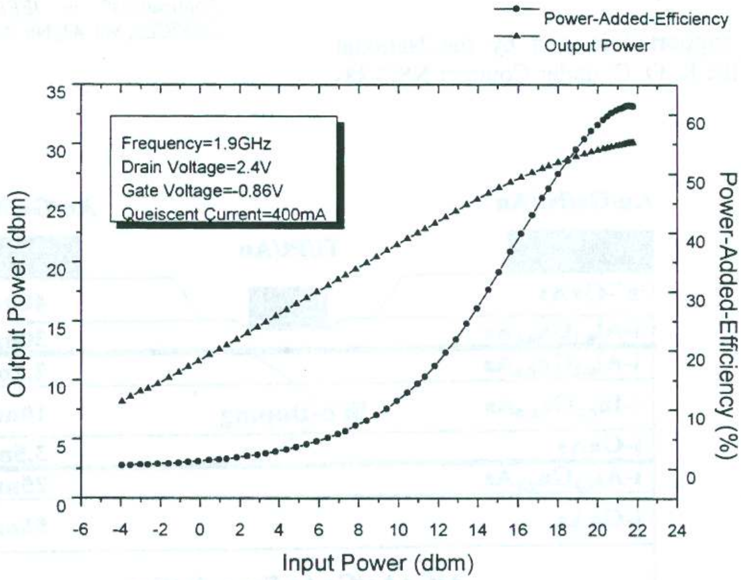

Fig. 4 Output power and power-added efficiency as a function of input power for the 20.16-mm GaAs power HEMT.

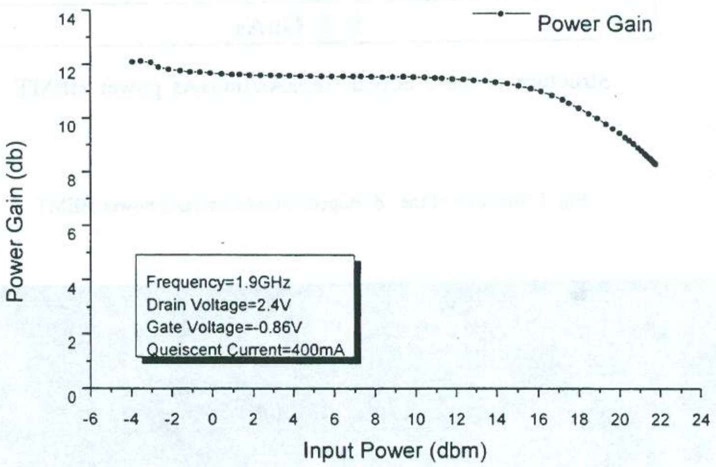

Fig. 5 Power gain as a function of input power for the 20.16-mm GaAs power HEMT.