A NOVEL APPROACH TO SCALABILITY FOR DISTRIBUTED FET MODELS

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Abstract - **A distributed CAD-oriented model for micro- and millimetre-wave FETs is presented along with a new scaling approach where number and width of the gate fingers are taken into account. Model identification is carried out through electromagnetic simulation of the device layout and conventional S-parameter measurements, without need of cumbersome optimisations. Experimental results confirm the validity of the proposed approach.**

I. INTRODUCTION

Distributed CAD-oriented approaches for the modelling of active devices as well as global design procedures where not only the values of passive (lumped or distributed) components, but also the active device geometry (e.g., number of fingers and gate width) represent available design parameters, would be very useful tools for the development of high performance, Micro- and Millimetre-wave Monolithic Integrated Circuits [1]. In this context, robust scaling procedures for FET models become an extremely interesting aspect to investigate. In the paper, a new approach to FET model scaling for MMIC design, which is based on an empirical distributed model [2..5], is proposed.

II. THE SMALL-SIGNAL DISTRIBUTED FET MODEL

The electron device is assumed to consist of an *"extrinsic passive network"* connected with a finite number of elementary *"active slices"* as shown in Fig.1. This description is intuitively suggested by the structure layout of a conventional FET. According to this description, model identification is conducted by means of a two-steps procedure, consisting of a distributed characterisation of the extrinsic passive part and a following extraction of the scattering matrix of the intrinsic active slices.
More precisely, the active part of the electron device is partitioned along each gate finger in a suitable number of active sections (represented by the FET symbols) which are interconnected by means of internal ports to the extrinsic passive network.
The number of active sections which must be considered, strongly depends on the device geometry and operating frequency range. Many authors adopt the approximate dimension $\lambda_g/10$ (λ_g being the electrical wavelength) as the upper limit above which distributed effects must be accounted for and as a thumb rule to introduce the proper number of active slices along the gate metallisation.
The passive structure, including "internal" ports for the three-terminal intrinsic active slices, is characterised through its scattering matrix $\underline{S}$ (see Fig.1), which is computed by means of electromagnetic simulation on the basis of layout geometry and material parameters (usually available from the design rules and provided by the foundry). Thus, since electromagnetic propagation and coupling effects are accounted for by the passive structure, all the active slices are described by the same three-port scattering matrix $\underline{\beta}_{AS}$, which can be identified, as will be shown in the following, once the scattering matrix $\underline{\alpha}$ of the whole electron device has been measured. It is worth noting that model identification does not require either parameter optimisation or complex measurements.

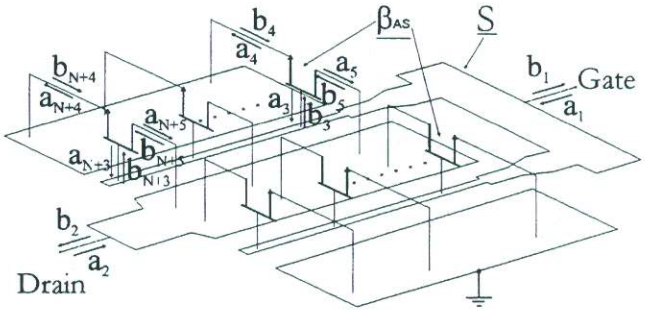


Fig.1: - Structure of the distributed model.

Clearly, in the identification procedure outlined above, the important assumption is made that current transport along the channel does not substantially affect the

characterisation of electromagnetic field distribution in the passive structure. In particular, just undoped GaAs was assumed to be under the metal structure. Moreover, also having the active part of the electron device "concentrated" into a limited, finite number of active slices, clearly represents an approximation[1]. These simplifications, which make it possible to use a conventional, commercially available electromagnetic simulator for model identification, cannot be easily justified by purely theoretical considerations. However, the results provided in the following show that the errors introduced by the above assumptions are not so relevant for electron device scaling. In particular, the next Sections will show how an equivalent Y-matrix per unit width of the electron device can be introduced and used to predict how electrical characteristics scale with gate width and number of fingers or, more generally, with device geometry variations.

Considering more in detail the identification of the matrix $\underline{\beta}_{AS}$, which describes each of the 2N active slices, we can introduce the vectors $\vec{a}_i$ and $\vec{b}_i$ whose elements are the incident and reflected waves at the ports of the i-th active slice, as shown in Fig.1. The symmetry of the device structure[2] introduces a linear dependence between rows and columns in the scattering matrix $\underline{S}$ whose dimensions are $[2+(2\cdot 3N)]\times[2+(2\cdot 3N)]$. These linear dependent rows and columns are eliminated in order to obtain a reduced scattering matrix $\underline{\tilde{S}}$ whose dimensions are $[2+(3N)]\times[2+(3N)]$. Moreover, after simple matrix manipulations, it is possible to write:

$$\begin{bmatrix} \vec{b}_1 \\ \vec{b}_2 \\ \vdots \\ \vec{b}_{N-1} \\ \vec{b}_N \end{bmatrix} = \underline{\tilde{S}}_1 \cdot \begin{bmatrix} (\underline{\alpha}-\underline{\partial})^{-1}\cdot\underline{\gamma} \\ \underline{I} \end{bmatrix} \cdot \begin{bmatrix} \vec{a}_1 \\ \vec{a}_2 \\ \vdots \\ \vec{a}_{N-1} \\ \vec{a}_N \end{bmatrix} \qquad (1)$$

where $\underline{\alpha}$ is the measured 2x2 scattering matrix of the electron device, $\underline{I}$ is a $(3N)\times(3N)$ identity matrix and the other matrices are obtained from $\underline{\tilde{S}}$ according to the following definitions:

$$\begin{aligned} \underline{\tilde{S}}_{i=1,3\cdot N\,;\,j=1,..2+3\cdot N} &= \underline{\tilde{S}}_{i=3,2+3\cdot N\,;\,j=1,.,2+3\cdot N} \\ \underline{\partial}_{i=1,2\,;\,j=1,2} &= \underline{\tilde{S}}_{i=1,2\,;\,j=1,2} \\ \underline{\gamma}_{i=1,2\,;\,j=1,..3\cdot N} &= \underline{\tilde{S}}_{i=1,2\,;\,j=3,.,2+3\cdot N} \end{aligned} \qquad (2)$$

By noting that (see Fig. 1) the scattering matrix $\underline{\beta}_{AS}$ associated with each active slice is defined as:

$$\vec{a}_i = \underline{\beta}_{AS}\cdot\vec{b}_i \qquad i=1,...N \qquad (3)$$

and defining the matrix $\underline{M}$ as:

$$\underline{M} = \underline{\tilde{S}}_1 \cdot \begin{bmatrix} (\underline{\alpha}-\underline{\partial})^{-1}\cdot\underline{\gamma} \\ \underline{I} \end{bmatrix} \qquad (4)$$

it is possible to obtain from (1) a homogeneous system of equations[3]:

$$\left(\underline{M}^{-1} - \underline{\tilde{\beta}}_{AS}\right)\cdot\begin{bmatrix} \vec{b}_1 \\ \vec{b}_2 \\ \vdots \\ \vec{b}_N \end{bmatrix} = 0$$

where :

$$\underline{\tilde{\beta}}_{AS} = \begin{bmatrix} \underline{\beta}_{AS} & 0 & \cdots & 0 \\ 0 & \underline{\beta}_{AS} & \cdots & 0 \\ \vdots & \vdots & & \vdots \\ 0 & 0 & \cdots & \underline{\beta}_{AS} \end{bmatrix} \qquad (5)$$

The necessary condition which guarantees the existence of a non-null solution of system (5) is:

$$\det\left(\underline{M}^{-1} - \underline{\tilde{\beta}}_{AS}\right) = 0 \qquad (6)$$

which can also be written in the form:

$$\det\left(\underline{I} - \underline{M}\cdot\underline{\tilde{\beta}}_{AS}\right) = 0 \qquad (7)$$

This latter is an eigenvalue problem, which can be solved in terms of $\underline{\tilde{\beta}}_{AS}$ by means of different available routines. For operating frequencies which are not extremely high and for electron devices having just two gate fingers, the case N=1 assumes particular importance as will be shown in the following. In that case the solution of problem (7) is simply:

[1] For these reasons, in the proposed empirical model, the *"active slices"* do not simply describe the active area of the electron device, but actually include all the errors associated with the above assumptions.

[2] A symmetric structure is very common in all high frequency devices.

[3] Equation (5) holds, provided that the matrix $\underline{M}$ is non singular, as in practice happens.

$$\underline{\beta}_{AS} = \underline{M}^{-1} \tag{8}$$

While in the case of N=2 a compact formulation can be derived:

$$\left(\underline{\beta}_{AS} - \overline{N}_{11}\right)\overline{N}_{21}^{-1}\left(\underline{\beta}_{AS} - \overline{N}_{22}\right) = \overline{N}_{12} \tag{9}$$

where the matrices $\overline{N}_{ij}$ with i, j = 1,2 represent the minors of $\underline{M}^{-1}$ defined in the following way:

$$\underline{M}^{-1} = \begin{bmatrix} \overline{N}_{11} & \overline{N}_{12} \\ \overline{N}_{21} & \overline{N}_{22} \end{bmatrix} \tag{10}$$

The numerical solution of Eq. (9) leads to the characterization of the intrinsic device in terms of scattering matrix. By means the conventional transformation it is possible to release the intrinsic device in terms of admittance matrix and then, if required, as equivalent circuit.

III. The new scaling approach

On the basis of the "intrinsic active slice" concept, a new scaling approach can be defined for families of devices sharing the same technology process (channel length, material stratification, doping profiles, etc.) but featuring different geometries (number of gate fingers, width of the gate finger, different structures for terminal access, etc.). In fact, provided that some scaling rules apply for the intrinsic active slice, any device of the assigned family can be modeled by means of the same (properly-scaled) active slice and the S-matrix of the relative passive structure.

As far as the scaling rule for the active slice is concerned, using a more convenient description in terms of equivalent admittance matrix $\underline{Y}_{AS}$ associated to a slice width W_{AS}, the following linear model is adopted:

$$\underline{Y}_{AS}(\omega, Vgs, Vds, W_{AS}) = \hat{\underline{Y}}_{AS}(\omega, Vgs, Vds) \cdot W_{AS} + \underline{C}(\omega, Vgs, Vds) \tag{11}$$

where $\hat{\underline{Y}}_{AS}(\omega, Vgs, Vds)$ and $\underline{C}(\omega, Vgs, Vds)$ are suitable 3x3 matrices to be identified. The offset matrix $\underline{C}$ in Eq. (11) takes into account possible effects, which are independent of gate width, as suggested by experimental evidence.

According to Eq. (11), the admittance matrices $\underline{Y}_{AS}$ associated with two electron devices having different gate widths are sufficient to identify the matrices $\hat{\underline{Y}}_{AS}$ and $\underline{C}$ at each frequency and bias condition. In practice, since Eq. (11) is in any case an approximation, we found that better prediction capabilities are obtained by evaluating the matrices $\hat{\underline{Y}}_{AS}$ and $\underline{C}$ on the basis of a linear regression applied to device structures covering a wide range of gate widths.

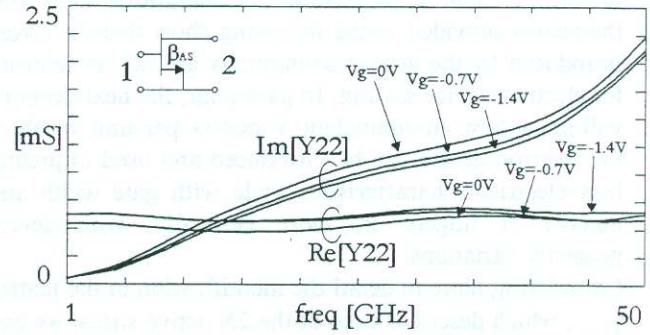


Fig.2 - Real and imaginary part of the output conductance of the intrinsic active slice (W_{AS}=50 μm).

The frequency dependence of the output admittance shown in Fig.2 allows for a phisically consistent interpretation of the output admittance in terms of parallel conductance and capacitance elements. Moreover, the small bias dependence of the real part of the output admittance is mainly due to the biasing condition in the saturation region (Vds=3V), while the imaginary part is consistent with an almost bias-independent drain-source capacitive behaviour.

IV. Experimental results

Different structures of GEC-Marconi F20 GaAs MESFET devices were measured and simulated to validate the proposed approach. More precisely, the scattering matrices of the extrinsic passive structures were computed, on the basis of foundry process parameters and device GDSII files, using the "em" Sonnet electromagnetic simulator [6]. The scattering parameters of the electron devices were measured directly on wafer up to a frequency of 50GHz using an HP8510C network analyzer. Moreover, the model was implemented in the HP-MDS program for microwave circuit design.

According to the procedure outlined above, model identification was carried out using three MESFET structures: a 2x25 μm, a 2x75 μm and a 2x150 μm device of the same wafer die, so that process dispersion is practically negligible. Moreover, a single slice per finger

was considered. This choice, which is not in contrast with the distributed nature of the modelling approach, has been found suitable up to 50 GHz.

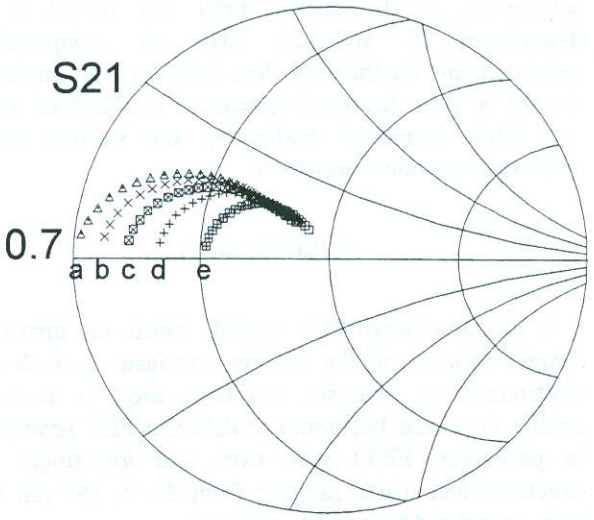


Fig.3 - Forward transmission S-parameter of the intrinsic active slice (W_{AS}=50 μm) for different bias conditions (a: Vgs=0V; b: Vgs=-0.35V; c: Vgs=-0.7V; d: Vgs=-1.05V; e: Vgs=-1.4V; Vds=3V).

Figs. 2-3 show the output admittance and the forward transmission S-parameter for the extracted active slice (for W_{AS}=50μm) at different bias conditions (for a more phisical interpretation of Figs.2-3, the active slice description has been converted from three- to two-ports, considering a "common" source configuration).

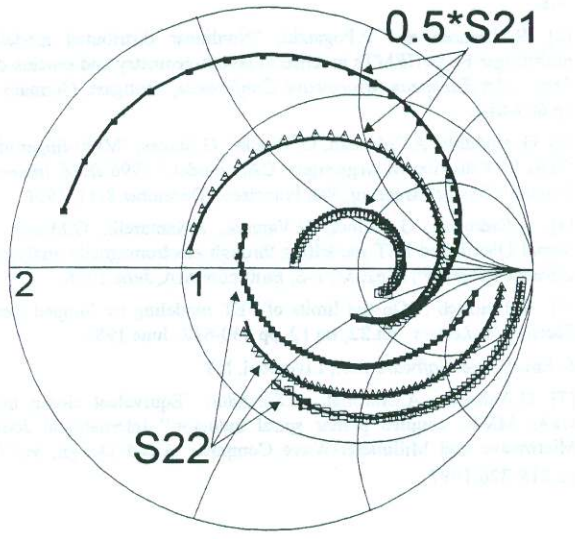


Fig.4 - Measured (symbols) and simulated (lines) S21 and S22 for three different FETs: filled box: 2x150 μm; triangle: 2x75 μm; empty box: 2x25 μm.

A first validation of the distributed FET model is presented in Fig.4, where measured and simulated S22 and S21 parameters are reported for the three devices used in the identification phase at the bias point Vgs=0V, Vds=3V. The good agreement confirms the high level of accuracy even when a simple linear regression is adopted for model scaling.

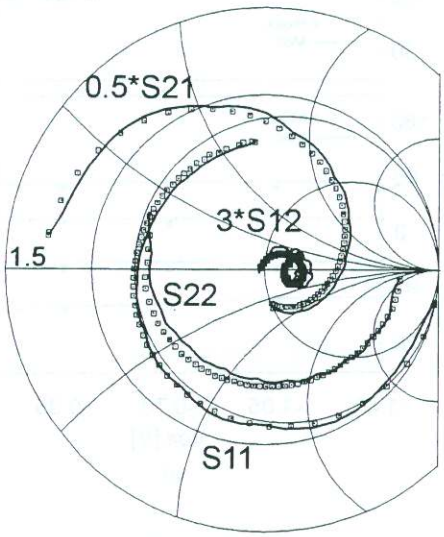


Fig.5 - Measured (box) and predicted (-) S-parameters for a 4x50 μm FET (Vgs=0V, Vds=3V).

Morover, in order to test the actual predictive capabilities of the scaling approach, the model was adopted to predict, on the basis of the active slice characterisation previously obtained, the small-signal behaviour of a 4x50 μm device (a structure which is strongly different from those used in the identification phase).

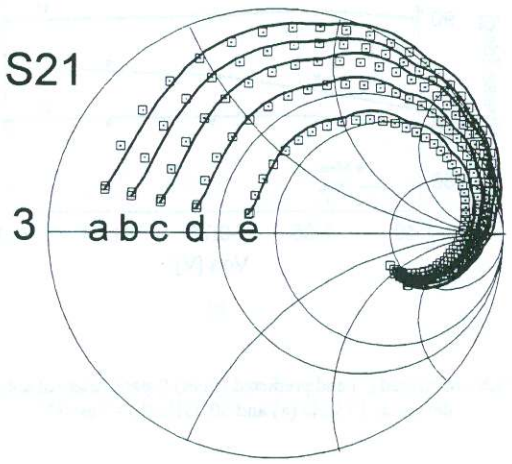
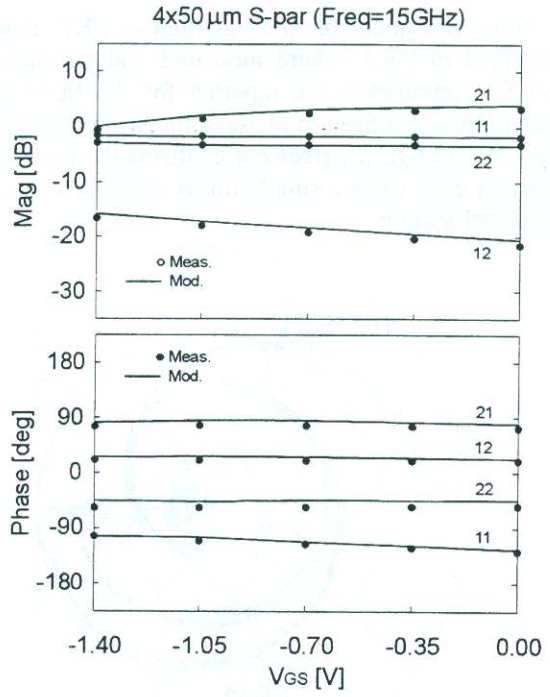


Fig.6 - Measured (box) and predicted (-) S21 parameter for a 4x50 μm FET for different bias conditions (a: Vgs=0V; b: Vgs=-0.35V; c: Vgs=-0.7V; d: Vgs=-1.05V; e: Vgs=-1.4V; Vds=3V).



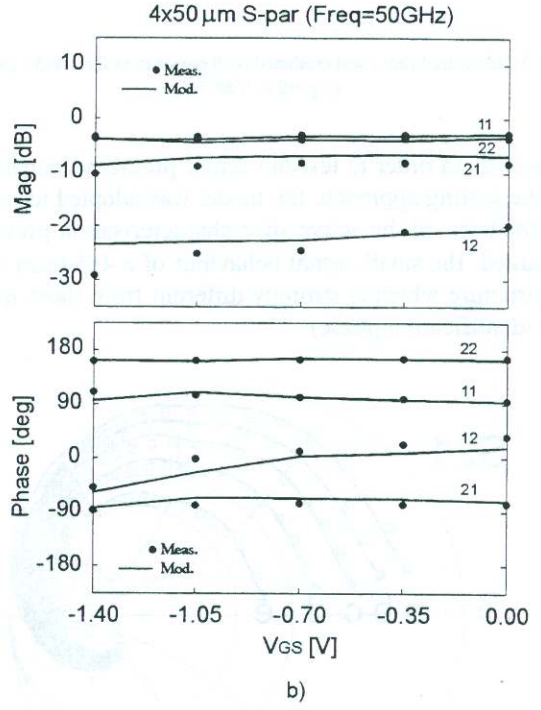


Fig.7a,b - Measured (*) and predicted (lines) S-parameters of a 4x50 µm device at 15 GHz (a) and 50 GHz (b) - Vds=3V.

Fig. 5 shows the measured and predicted S parameters for the 4x50 µm GaAs MESFET, in the same bias point as Fig. 4. Similar comparisons have been conducted also for other bias conditions. For example, in Fig. 6, the S21 parameter of the 4x50 µm device is shown for five different biases, ranging from pinched-off to fully open channel conditions. Finally, in Fig. 7 the predicted S-parameters of the scaled 4x50 µm device at the frequencies 15 and 50 GHz are compared to measurements for the same five different bias conditions. As can be seen, the good agreement is preserved also at very high frequency confirming the validity of the proposed distributed approach.

V. Conclusion

A CAD-oriented FET model, based on distributed characterisation of the passive extrinsic part through electromagnetic analysis, has been used to accurately predict the linear behaviour of different FET geometries. In particular, FETs with two- and four-finger gate structures and width ranging from 25 to 150 µm have been considered for model validation.

The distributed characterisation of the extrinsic structures is found compatible with a phisically consistent extraction of intrinsic "active slice" components.

The presented approach will be extended to predict also the nonlinear dynamic FET behaviour.

VI. References

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