

Design of a Broadband Amplifier for High Speed Applications

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This paper provides comprehensive insight into the design approach followed for an amplifier dedicated to high speed base band signals. To demonstrate the methodology, an amplifier consisting of nine PHEMT cascode cells within a distributed amplifier topology was designed. The resulting frequency response is 40 GHz at the 3-dB point, and the output voltage for a 43 Gbps eye diagram is 7.3 Vpp at the chip terminal.

INTRODUCTION

The advent of optical transceivers operating at 40 Gbps is creating the need for very sophisticated components. In particular, the amplifier used to drive the modulator is required to present cutting-edge performance such as frequency bandwidth greater than 30 GHz and an output power of +20 dBm. In addition, the amount of gain necessary to amplify the MUX input signal to the level required by the crystal modulator is commonly between 25 to 30 dB [1]. Several publications have already addressed these issues [2] & [3], and MMICs specially designed for this market are becoming available [4]. The present paper discusses the issues involved in the design of a distributed amplifier for this application. The amplifier uses Fujitsu's 0.15 μm gate length double heterojunction PHEMT technology to achieve a high current density and high f_T previously described in [5]. This design resulted in a state-of-the-art component to be readily inserted into 40 Gbps modulator driver modules.

DESIGN APPROACH

In high speed applications there are a set of parameters that are not usually considered in conventional MMIC amplifier design. Besides gain and bandwidth, the designer must understand jitter, delay response, pulse width distortion and, most of all, guarantee that the eye diagram at the amplifier output is open. The first set of parameters can be controlled in frequency domain design methodology, but the latter requires the use of empirical time domain techniques.

Bandwidth—A series of simulations were carried out for different types of filter responses to represent typical amplifier small-signal frequency response. The minimum bandwidth for an open eye condition, considering a digital baseband signal, was obtained for ideal Gaussian (or Bessel) response, and is equal to $BW = B/2$, where B stands for data rate. That condition is shown in Fig. 1 depicting the effect of

limited bandwidth on the output signal. Under this ideal assumption, a digital NRZ signal will be distorted at the output, but an open eye diagram is obtained. Simulations showed that responses tailored to Butterworth or Chebyshev introduces intersymbol interference for the same cutoff frequency. An amplifier with such frequency response can only be used if it shows a higher cutoff frequency. Under this condition, simulations showed the eye diagram is open but there will be a certain degree of overshoot in the output waveform. This is an important property since in real millimeterwave amplifiers it is difficult to properly control the frequency response.

The eye diagrams represented in Fig. 2 clearly shows that there is no margin for jitter when a limited bandwidth is used. Therefore, a larger bandwidth is required to guarantee an open eye. A common rule of thumb is to use an amplifier with a slightly larger bandwidth, say $BW' = 2B/3$. The actual MMICs must possess a bandwidth higher than BW' , to take into account the degrading effects of bias and decoupling circuits when they are inserted into driver modules. Therefore, the bandwidth requirement depends on the module technology used as well as the semiconductor technology. For this application, the target bandwidth was >40 GHz at the 3 dB point.

Linear and Non-linear operation—In the linear mode of operation, the first concern is flat gain and linear phase. The latter translates into a constant and low phase delay response. The time domain effect of the amplifier can be easily obtained from ADS simulation. The second concern is on jitter degradation arising from the amplifier noise figure and from mild nonlinearities that contribute to eye closure. The third concern is on the performance degradation due to temperature. Unfortunately these effects cannot be effectively predicted with present electrical simulators. When the amplifier operates under non-linear conditions, some benefits are expected. Under saturation, the amplifier functions as a limiter so that

small amplitude variations are leveled and the frequency response improves. For the same reason, the gain becomes less temperature dependent, and the amplifier is capable of sustaining larger peak-to-peak voltage on a 50-ohm load. The rise time also improves due to the clipping of the waveform. Unfortunately, the drawback of driving the amplifier into saturation is a higher AM to PM conversion, which degrades the jitter performance. The non-linear simulation under single-tone excitation was used to estimate the power performance at the bit rate frequency. However, the time domain analysis using available harmonic balance simulators, was not efficient, resulted in frequent convergence problems, and the design had to be done using empirical techniques.

Device Technology—The FET construction has been previously reported [5], and its main parameters are listed in Table I. The high transconductance and high cut-off frequency offered by this technology enable operation at high power with low power dissipation. Load-pull evaluation carried out at 26 GHz for these devices showed each $W_g = 100 \mu\text{m}$ device can provide $P_{1\text{dB}} = +12 \text{ dBm}$ with a maximum available gain of 15 dB when biased at $V_{\text{DD}} = 3.5 \text{ volts}$ and 60% I_{DSS} .

AMPLIFIER DESIGN

The distributed amplifier approach is employed in this design for its proven performance over large bandwidths. The design consists of nine cascode cells, which are well known for their high input-to-output isolation. A higher output voltage is available from this configuration compared to single-ended common-source topologies, using narrow gate length devices. A schematic of one cascode cell is shown in Fig. 3. The impedance Z_{g2} is of major importance in the design. At low frequencies it is resistive absorbing the excess low frequency gain of the devices. At high frequencies it is used to generate a small amount of negative resistance, therefore compensating losses in the gate and drain lines. The impedance Z_{d1} is used to control amplifier stability in addition to helping shape the amplifier response.

This topology plus the input and output transmission lines were computer optimized to obtain a flat gain up to 40 GHz. Besides the amplitude response, the optimization process weighted the effect of phase linearity. As a matter of fact, the negative resistance compensation had to be sacrificed for better phase response. The power capability of the cascode cell is reduced under these circuit conditions, according to single-tone 20 GHz large-signal simulation. To make this amplifier capable of operating at low frequencies, say 50 kHz, the gate and drain terminations need to be specially designed. On the gate side, a simple 40-ohm load connected to ground via a 2 pF capacitor provides good performance to frequencies near 0.5 GHz. Below

that frequency, the gain response is determined by off-chip components. An association of a 10-ohm series resistor and high value chip capacitors provided the required flat 3 dB gain response. The gate is biased through this resistance. On the drain side, a similar arrangement was employed, but bias had to be applied through an external bias tee because the amount of current is prohibitively large to be applied through an epitaxial resistor. The amplifier was designed for a 28 μm substrate thickness. This structure results in a very low thermal resistance, improving the thermal performance and contributes to a smaller chip design. It also eases the use of inductive lines, key to distributed amplifier design, at the expense of higher circuit losses.

RESULTS

In order to perform small-signal and large-signal MMIC evaluation, each chip was mounted on a carrier with AuSn solder. External bypass components were wire-bonded to the gate and drain terminations to control the low-frequency response. Each MMIC was then measured using GSG wafer probes at the RF input and RF output pads, where the gate and drain biases were applied through bias tees. The device was biased at the target bias point of $V_{\text{DD}} = 7 \text{ V}$ and $I_{\text{DD}} = 240 \text{ mA}$. The small-signal amplifier gain response of 13 dB is shown in Fig. 4, which compares favorably to the simulated results up to 40 GHz. The gain ripple is less than 0.5 dB to 30 GHz. There are some discrepancies above 40 GHz due to inaccuracies in the model at very high frequencies. The amplifier delay response (shown in Fig. 5) is $75 \pm 15 \text{ ps}$ over most of the frequency band. The measured input and output match is better than 10 dB within the band. The large signal performance at 20 GHz is shown in Fig. 6 as a function of drain voltage. The plot shows a maximum output power $P_{3\text{dB}}$ of +22.7 dBm controllable down to +19.2 dBm for a drain voltage of 3.0 V. In order to perform time domain evaluation at 43 Gbps, 50-ohm alumina substrates were mounted on the carriers. These 0.005" thick substrates were double wire-bonded to the RF input and RF output pads of the MMICs. The carrier was then placed on a fixture with high frequency launchers contacting the substrates. Each launcher has a frequency dependent loss of approximately 0.5 dB at 20 GHz.

A special time domain waveform was used to test the amplifier. It consisted of applying a 16-bit sequence of six 1's followed by a sequence of six 0's then 1010 at the highest specified data rate. Observing the output waveform shown in Fig. 7, it was possible to verify the amplifier time response. The long sequences showed an amplifier free of parasitic oscillations and some ringing due to transmission line propagation. A low overshoot was also observed right after the low-to-high transition. The alternating 1010 is about of the same

level as the long sequences—a sign of uniform compression over the frequency band. The eye diagram was taken for a $2^{31}-1$ pseudorandom bit pattern, provided by a SHF pattern generator. Under small-signal operation, there was no noticeable effect on the eye diagram. To obtain the maximum voltage on the output load, the device was compressed, and the input and output eye patterns are plotted in Fig. 8. Limitations of the input signal quality are observed in the form of alternating eye degradation, but the voltage swing of the amplified signal is around 7.3 volts, which is a remarkable value at 43 Gbps. The observed jitter contributed by the MMIC is minimal for this output voltage. Evaluations were also done at lower drain voltages and down to 4 volts bias, showing a good eye opening and a small degradation on jitter, resulting from higher compression operation.

CONCLUSION

A MMIC distributed amplifier with 40 GHz bandwidth at the 3 dB point has been developed which is capable of delivering an output voltage swing of 7.3 Vpp. The results presented also show the effect of compressed operation upon the eye diagram for the chip.

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TABLE I
SUMMARY OF DEVICE PARAMETERS

$g_{m,max} = 525$ mS/mm	$L_g = 0.15$ μ m
$V_{th} = -0.9$ volts	$f_T = 90$ GHz
$V_{gdo} = 7$ volts	$f_{max} = 130$ GHz
$I_{DSS} = 310$ mA/mm	$R_{th} = 165$ °C/W

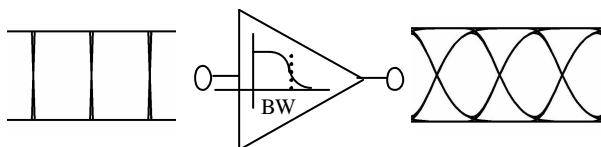


Fig. 1. Filter with Gaussian 3-dB bandwidth of $BW = B/2$

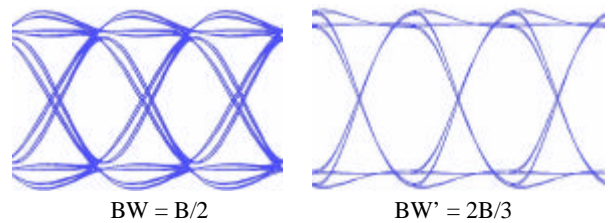


Fig. 2. Effect of 3-dB bandwidth on jitter and eye diagram for a Butterworth filter with ideal input signal

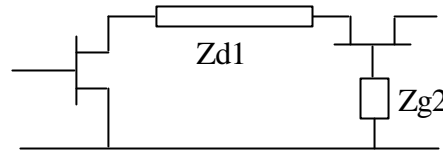


Fig. 3. Detail of cascode cell

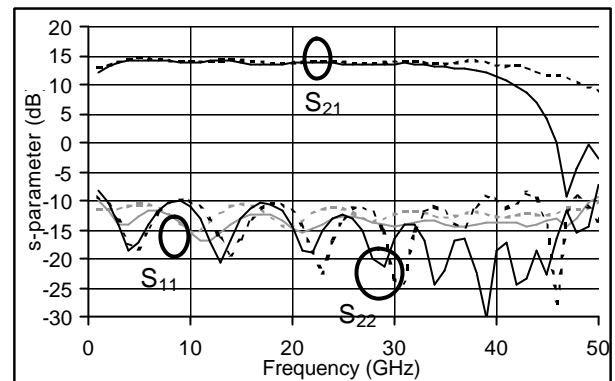


Fig. 4. Measured (—) and simulated (---) small-signal s -parameter results for the driver MMIC chip ($V_{DD} = 7$ V and $I_{DD} = 240$ mA)

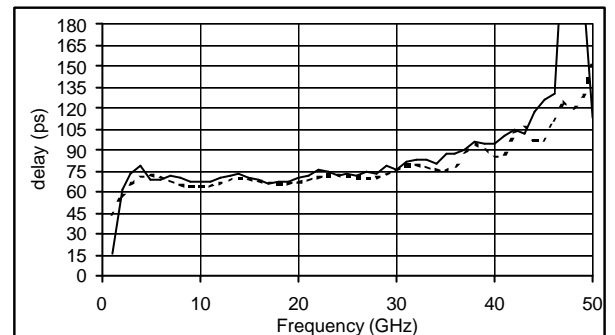


Fig. 5. Measured (—) and simulated (---) group delay results for the driver MMIC chip ($V_{DD} = 7$ V and $I_{DD} = 240$ mA)

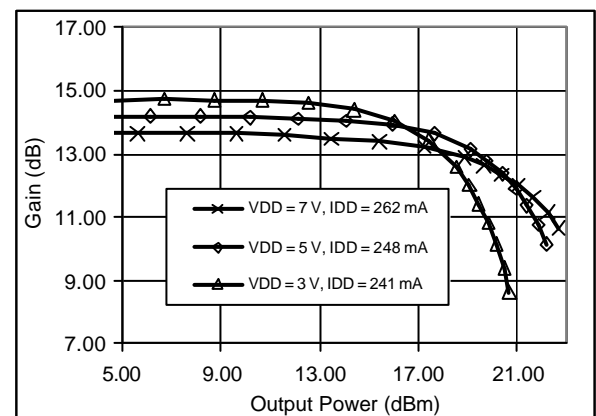


Fig. 6. Measured gain compression as a function of output power and bias for the driver MMIC

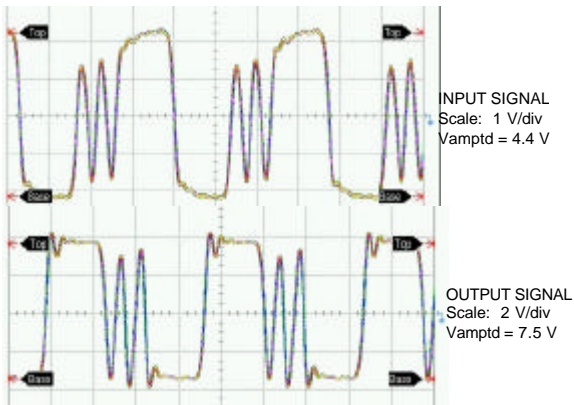


Fig. 7. Measured input and compressed mode output 43-Gbps 16-bit pattern results for the driver MMIC ($V_{DD} = 7$ V and $I_{DD} = 220$ mA)

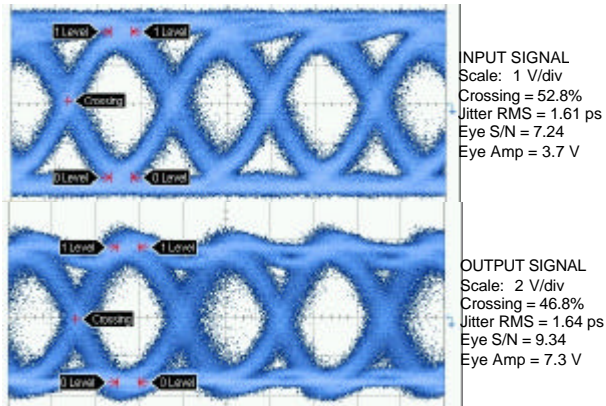


Fig. 8. Measured input and compressed mode output 43-Gbps eye diagram results for the driver MMIC ($V_{DD} = 7$ V and $I_{DD} = 220$ mA)