THE POWER AMPLIFIER RAT RACE FOR DIGITAL MOBILECOM APPLICATIONS

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ABSTRACT

With more than 100M cellular and cordless phones already this year, the digital mobilecom market is booming rapidly attracting a lot of interest from CMOS and BiCMOS IC suppliers wanting to grab a big share of it. Yet, the high power amplifier (> 1 W) in the transmit chain, because it cannot easily be integrated in mainstream Si processes, remains a battlefield for GaAs and Si technologies with no clear winner so far. Power added efficiency at high and low power levels and low supply voltage, device count, cost, reliability as well as ease of power control are the key parameters which are governing the power amplifier rat race.

INTRODUCTION

For the first time, the traditional professional microwave telecommunication market is becoming a consumer market with more than 100 Million portable phones to be sold in 1998 and more than 200 Million phones a year in 3 years' time. This is also the first time that the system needs especially the RF part of the mobile phones are ahead of what the most advanced technologies can offer. One can speak of "system push" replacing the usual "technology push". This is achieved by asking more from the technologies as never before in terms of performance and low cost. In particular advances in base band CMOS ICs and BiCMOS RF receiving ICs clearly enable to integrate more and consume less . The ultimate goal is to demonstrate the feasibility of a ONE CHIP mobile com terminal.

However the power amplifier (PA) in the transmit chain has until now been a separate function: suppliers of PAs in various processes like GaAs MESFETs, PHEMTs, GaAs HBTs and Si BJTs, Si HBTs and finally Si LDMOS are fighting hard to win the phone makers over. In this paper we will review why this function is difficult to integrate and will remain for a long time a limiting factor to the phone talk time, the ease of production and cost. After discussing the PA specifications in terms of mobilecom standards and system partitioning, we will see how the various technologies match the needs.

The partitioning issue leading to the Power Amplifier rat race : Basically, portable digital phones and portable multimedia terminals in the future are developed at the pace of a new generation every year. The key drivers for new phones are clearly today :

- Low price : The retail prices today are dropping every year by 20 to 30 % depending on the standard
- Small size and low weight : Although there might be a physical limit as well as cultural differences across the world, phones below 100 cm^3 and 100 g are now available and 50 cm^3 50 g will be achieved within 4 years from now.
- Talk time and stand-by time: most phones offer today about 1 day use (with 10 % talk time) and 2 to 3 day use is possible in the coming years.
- More features including data transmission and multiband / multi mode capabilities which will lead to multimedia terminals and the use of more linear digital modulation like in the W-CDMA standard.

In order to meet these needs, the name of the game is again as much integration as possible in full CMOS processes.

A large portion of the phone ICs can be implemented in CMOS processes like the LCD drivers or in advanced 0.25 µm CMOS like the DSP blocks in the base-band section (fig 1).The CMOS tidal wave has not been able so far to reach the RFsection of the terminal which is mainly dominated by 0.5 µm BiCMOS especially for the downconverters, the PLLs and the upconverters. GaAs ICs are sometimes used in the receivers of TDMA and CDMA phones in the US or PDC phones in Japan when high linearity LNAs and mixers are needed. Finally RF CMOS is a highly debated topic which is getting out of the university labs and is now seriously considered by the major RFIC suppliers.

The power amplifier function (PAF) in the transmit chain is still a stand-alone function getting more and more attention from the system engineer since it burns up to 40 % of the total phone current (table 1). The main reason is that advanced digital CMOS and BiCMOS processes do not have the right breakdown voltage to generate high power levels above a few hundreds of mW up to 2 GHz and in addition in a single chip transceiver the large voltage swing in the PA would strongly degrade the phase noise performance of the receiver through substrate leakage. The power amplifier function not only includes a power amplifier but also when power level control is needed, a power level detector, a comparator and power level references (fig 1) which are supplied by the base-band section.

When an architecture is defined the partitioning between the various IC technologies is key to meeting the targeted terminal specifications.

Almost all the digital US and Japanese cellular phones (DAMPS, CDMA, PDC) use GaAs MESFET, PHEMT or HBT ICs for the PA while digital European cellular phones (GSM, DCS) use mainly Si BJT line-ups, Si BJT or LDMOS power modules at 900 Mhz and GaAs MMICs especially at 1800 MHz. GSM and DCS phones are now the most severe PA battlefield mainly because this represents about 50 % of the total market and will continue to be so in the coming years.

The PA performance and technologies to match : Digital phones require high power PAs from 800 MHz to 2 GHz with supply voltages ranging from 4.8 V to 2.4 V. The maximum output power varies from 35 dBm for GSM to 25 dBm for DECT. The duty cycle which is critical in terms of thermal behaviour is 100 % (CW operation) for CDMA and as low as 12.5 % for GSM/DCS (table 2). The PA is generally specified up to 70°C ambient temperature. Leakage current of the PA in the stand-by should be negligible with respect to that of the base-band section (including timing) which is expected to drop to less than 3 mA when 1.8 V CMOS processes are used.

The power control loop and the off leakage current : these two conditions are unexpectedly related. All silicon technologies can be turned off by grounding the PA input (this is obvious with BJT's but require a large enough Vt with LDMOSFETs to account for temperature variation). Consequently the power control is done by changing the DC biasing of the gate or base of the transistor. This is acceptable as long as the transfer gain (dB / V) is not too high which might happen at low power level. Except for HBTs and E-FET's, GaAs PAs require a drain switch (usually a low R_{on} MOSFET) to turn it off (fig 2). The drain switch can then quite naturally be used to control power with a smooth transfer curve.

The saturated output power, saturated power added efficiency spec (PAE) and the breakdown voltage of the transistors : some of the digital standards like GSM, DCS and DECT use a constant envelope modulation scheme which enables to over drive the amplifier in the mode (3 to 5 dB into saturation). This type of operation also referred to as class E or class F yields up to

100 % PAE if you can generate out of phase current and voltage pulses into the load (fig 3). This can be translated into process specifications like QV transistor knee voltage, a breakdown voltage larger than 4 times the supply voltage and a gain cut-off frequency more than 15 times the operating frequency.
GaAs FET or HBT processes can yield high breakdown voltage (>12 V) with a high cut-off frequency (> 30 GHz). This is not true of Si BJTs and Si HBTs where the product ft* breakdown voltage is quasi constant (150 GHz*V). Consequently 3 stage GaAs PAs achieve typically 55 % to 60 % PAE which is 10 % more at 900 MHz than their Si counterparts. However, this high performance is only available if a manufacturable output matching network can be designed with negligible resistive loss (high Q passive components) to reject 2nd and 3rd harmonics sufficiently (usually more than 45 dBc rejection is needed).

The linearity specification and the power added efficiency at nominal output power : Linearity is a key specification especially for non constant envelope modulation scheme like OQPSK (offset quadrature phase shift keying) and DQPSK (differential quadrature phase shift keying) used respectively in the CDMA and TDMA US digital standards. Some degree of amplitude modulation enables to achieve higher spectral density, however gain compression causes the carefully bandwidth limited signal to distort and spill over into adjacent channels. Linearity of the power amplifier is usually expressed in terms of IMD (intermodulation distortion) but for CDMA and TDMA, adjacent channel power rejection (ACPR) is preferred. ACPR of - 30 dBc up to - 55 dBc are required for TDMA and CDMA communications.
A second specification directly related to the linearity specification concerns the performance of the PA under nominal operating conditions. CDMA is an extreme case since the nominal power level is only 10 mW which is significantly lower than the maximum power level. The best PA will therefore combine :

- The most linear processes like GaAs PHEMT or HBT processes which exhibit IP3 / P-1dB ratio higher than 12 dB (IP3 is the third order intermodulation product and P-1dB is the output power at 1 dB gain compression).
- and a controlled drain power supply in order to dynamically adjust the DC bias point with the changing output power in order to maximize the power added efficiency (1). 10% PAE can thus be achieved at 10 mW Pout.

Nevertheless, linearity, Max output power and power added efficiency at various power levels are contradictory parameters which will always require refined optimization (2) specific to the targeted mobilecom standard.

The battery supply voltage : Recent advances in lithium ion batteries have made less than 100 cm^3 and 100 g 3V cellular phones possible. New base- band 1.8 V ICs will soon be available, but the receiver part is already struggling at 2.4 V and the PA output resistance can hardly be further reduced as long as an output power of 1 W or more is required. Here PHEMT processes have an edge over the others, with an increasing gain and ft as Vdd is dropped from 3 V to 1 V. This is not true with BJT or HBT processes, especially GaAs HBTs due to the high input turn-on voltage.

The device count and the packaging alternatives : It might be the most controversial parameter in the end. The amount of devices needed to implement the PA function typically varies from 10 to 40 depending on the standard and on the process used. Active and passive components are required for :

- input matching
- output matching
- interstage matching and decoupling

* power control (power sense, MOSFETs drain switch with GaAs FET PA's, on-chip negative voltage generation for MESFET PA's..)

Plug and play solutions are proposed in the form of a hybrid module. This does reduce the device count dramatically and the total area occupied by the PA function, but at the expense of the performance (lossy and cheap ceramic substrates are used). The high performance of MMICs are best preserved in a TSSOP package with metal plug mounted directly on the phone PCB.

Success stories :

All the major PA competing technologies have been designed-in in commercially available cellular or cordless phones and none can pretend to have won the rat race so far. This just proves that the final decision leading to a succesful design-in is based on criteria specific to the phone manufacturer and the type of phones :

* Premium tier phone or low cost phone : GaAs tends to be used for premium tier phone when the high PAE counts more
* US or European standard : GaAs PAs are more easily designed-in in US cellular phones when the linearity is an issue.
* Single mode plug -play power module : This has been the realm of Si LDMOS (3) and Si BJTs so far.

Some of the major successes of 3 V and 2 V GaAs MMIC PAs are found in DECT (fig. 4), GSM, DCS and CDMA phones as shown in table 3.

The near future :

Multimode multiband PAs : the first multiband phones appearing on the market, are using two separate PAs like in GSM900 MHz/DCS 1800 MHz phones. One chip dual band GaAs PAs have also been reported to offer the best trade-off between performance, cost and ease of use.The wide band behaviour of the PA itself makes it possible to achieve the multiband function with one chip only and two matching network at the output or at the input.The advantage of GaAs is here more pronounced because of the higher integration capability.

GaAs versus SiGe BiCMOS : SiGe BiCMOS is nothing else than one advanced generation of BiCMOS processes with the same breakdown voltage* cut-off frequency limitation as any bipolar processes. Current PA results show that for DECT applications at 3 V, 26.5 dBm Pout and PAE of 40 % are achieved which is about 20 % less than PHEMT PAs. Another severe limitation of present SiGe technologies is the power loss in the interconnects since* thick Gold interconnects are not readily available like in GaAs processes (4).

CONCLUSIONS

In the early 80's there was a fierce debate about the best high speed digital technology until full CMOS proved to be the winner especially because of its downscaling and high density memory capability. The present PA controversy is very much similar and will certainly continue until the RF CMOS tide sets in. For the time being, GaAs PA ICs will be used in a sizeable number of phones if it is recognized to be a fully proven consumer IC technology not only available from successful start ups.

Acknowlegments

I would like to thank all the GaAs IC product line personnel of Philips Semiconductors in Limeil and in Caen who are dedicated to proving that GaAs ICs are fully complementary to Si solutions.

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Figures

Figure 1 : Functional partitioning of a 900 Mhz mobilecom terminal
Figure 2 : GaAs FET PA with peripheral devices
Figure 3 : Ideal PA operation
Figure 4 : Performance of PHEMT PA for DECT(1.9 Ghz, Pin = - 5 dBm)

Tables

Table 1 : Power consumption breakdown in a mobile phone
Table 2 : Main cellular standards
Table 3 : Main 3V GaAs PA performance

	paging mode	speaking mode	total (80 % - 20 %)
RF	40 %	15 %	20 %
PA	0 %	50 %	40 %
Base-Band + Codec + timing	60 %	35 %	40 %

Table 1

standards	frequency (MHz)	modulation	acces mode	duty cycle	Pout max
GSM	900	GMSK	TDMA	12.5 %	2 W
DCS	1750	GMSK	TDMA	12.5 %	1 W
IS95	850 / 1900	OQPSK	CDMA	CW	200 mW
IS136	850 / 1900	DQPSK	TDMA	33 %	< 1 W

Table 2

standard	process	supply voltage (V)	Pout (nominal) (mW)	Pout (max) (mW)	PAE at Pout nominal (%)
DECT	PHEMT	2.4		400	65
GSM	HBT	3.6	3 000	3 500	60
DCS	MESFET	3.6	1500	2000	53
CDMA	PHEMT	3	10	500	10

Table 3

Figure 1

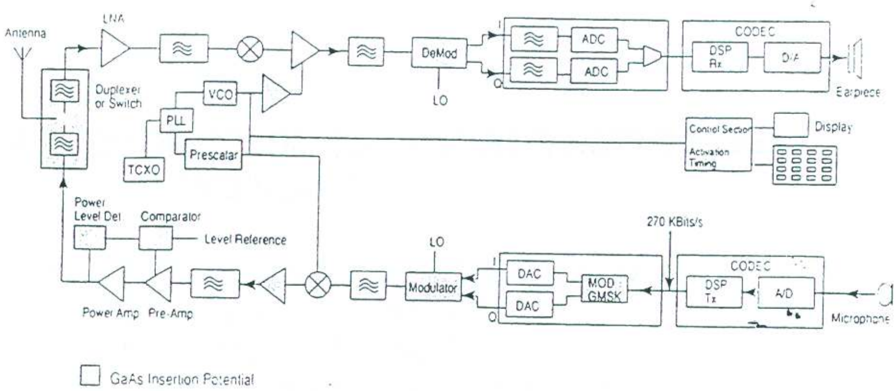
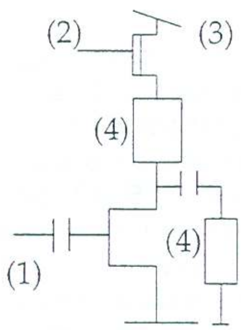


Figure 2



gate DC biasing (1) : >0 ou <0

Drain switch (2) : drain leakage

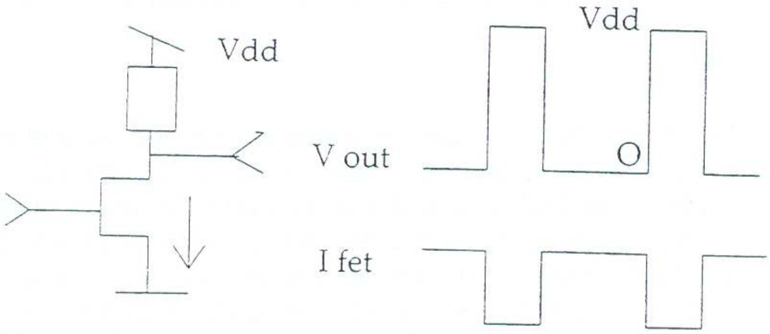
chip size : < 2mm2

Vdd (3) : down to 1V

PAE: > 60%

Board space :(1) + (2) + (4) + packaging

Figure 3



Pfet =0, Pload = P battery
(Fmax=20 F operation, knee voltage= 0V
lossless load)

Figure 4