MONOLITHIC LOW NOISE AMPLIFIER FOR X-BAND APPLICATIONS

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ABSTRACT

This paper presents the design aspects and performance of a monolithic low noise amplifier (LNA) for X-band applications. The LNA, based on GaAs PM-HEMT technology, shows a noise figure of only 1.1 dB at room temperature and a gain of 19 dB with high gain flatness over a bandwidth of 30%. The design was induced by the requirements of real active phased array antenna modes, e. g. switched applications, high IP3 and damage level. A statistical analysis over a large number of LNAs is added showing the high yield and good uniformity of this device.

INTRODUCTION

The development of Transmit/Receive (T/R) modules /1/ is driven by the growing demand on active phased arrays for ground, naval, airborne and space based radar systems for military and commercial applications. Such an antenna array consists of several hundred or thousand T/R modules. Key system parameters such as noise figure, spurious free dynamic range, spectral purity, power consumption and finally cost dictate most aspects of the design of a T/R module. One important element of such a complex T/R module is the low noise amplifier /2/ which influences a lot of these key system parameters, a fact which is often overseen or undervalued by the overall design. Besides the electrical performance of an individual LNA the primary challenges of the LNA design are reproducability, RF yield and low chip size (cost).

DEVICE TECHNOLOGY AND CHARACTERISTICS

Prior to circuit design the most adequate technology has to be selected. For chip processing the Daimler-Benz GaAs Center located in Ulm/Germany was selected (this foundry has merged with the Thomson-CSF semiconductors and now offers foundry services under the new name United Monolithic Semiconductors UMS). Among the variety of dedicated processes offered by the Daimler-Benz GaAs Center the 0.25 µm PM-HEMT was selected.

This process features GaAs/GaInAs FETs grown by MBE technology. The recessed gate structure allows best minimum noise figure of approx. 0.7 dB at 12 GHz and a f_T of 70 GHz. To control recess etching an etch stop layer is introduced. Thus a very good uniformity of device characteristics across the whole 3" wafer is possible. A silicon nitride passivation ensures stable and reliable circuits. Spiral inductors with airbridge crossovers, MIM capacitors, both epitaxial GaAs and sputtered tantalum thin film resistors and via holes complete the element library.

The typical DC characteristics (normalized to 1mm gate width) of the HEMTs are 250 mA/mm drain current and a pinch off voltage of about -0.8 V. Maximum transconductance is 600 mS/mm. Minimum noise figure is achieved at a drain current of 30% Idss. However the minimum is very flat: changing the bias between 10% and 50% Idss does not influence the noise figure dramatically. Output power at 1 dB compresson is approximately 21 dBm/mm.

CIRCUIT DESIGN

The principal aim of the design was to achieve excellent input- and output matching while still keeping the noise figure to a minimum value. In addition the power consumption was to be held as low as possible. For the given specification a two stage design was found to be appropriate. The first stage was to show a low noise figure and good match. The second stage designed to compensate the gain roll off of the first stage and to deliver the required output power at reasonable output match. In order to deliver the required output power the gate width must be at least 200 µm. Adding some margin a 240 µm HEMT (6 fingers @ 40 µm) was chosen. This size is also used in the first stage to make the input more robust to power overload. The current penalty is small as the first stage is operated at only 30 % Idss.

A well-known technique which allows simultaneous noise match and input match over a sufficiently broad bandwidth is the introduction of a source inductance. At X-band a small length of microstrip is sufficient. The length was determined by a trade off among noise figure, match and stability. An input matching network was selected which uses low loss series elements and one parallel element. The parallel element is also used for DC biasing.

To receive a good gain flatness the second stage must have a positive gain slope compensating the input stage. As the noise contribution of the second stage is divided by the gain of the first stage a lossy feedback in the second stage is possible (and needed). This is done by means of a RLC series network between the drain and the gate. The output network provides good match and biasing of the HEMT.

HEMTs of small gate lenghts show very high gain at low frequencies and tend to oscillate.

To stabilize the HEMTs, resistive networks in the drain connections are implemented. Capacitors in parallel lower the noise contribution of these resistors in the operational bandwidth.

The layout of the chip is shown in figure 1. Standard coplanar ports are used for RF connections, DC connections for the gate and drain voltages are aligned at one edege. The chip size is 2010 µm by 870 µm.

CIRCUIT PERFORMANCE

The amplifier was designed to operate from 8 GHz to 11.5 GHz. Broadband measurements show that the chips can be used over a broader bandwidth.

Figure 2 shows the characteristics of LNA. The measurements were taken on a wafer-prober at a bias of 5V and 50 mA. The curves show a very good noise figure of 1.1 dB at midband, a gain of 18.8 dB at ±0.15 dB ripple and excellent match. The S-parameters of HEMTs are more stable with respect to temperature than MESFETs. In figure 3 gain and noise measurements from a temperature sweep from 23°C to 100°C are depicted. Without any compensation circuitry the two stage LNA show -0.012 dB/°C gain degradation over temperature (a comparable MESFET amplifier would show approx. -0.030 dB/°C). The LNA delivers 12.5 dBm output power at 1 dB gain compression. The measurement results are compiled in Table 1.

For power-critical applications the chip may be operate with 3V and 15 mA drain current. Noise figure and match do not degrade, but gain and 1 dB compression point are lower (16 dB and 2 dBm respectively).

In most T/R module applications the LNA is switched off during transmit to decrease loop gain. Thus the switched performance of the chip is important and was measured. The switching time to ±0.5 dB from final value is about 30 nS when drain is pulsed.

For T/R module design, especially for the limiter performance, the knowledge of the LNA damage level is important. A detailed investigation was carried out concerning pulse recovery time and damage level of the chip. With a pulse width of 10 µS and a duty cycle of 10 % a damage level

above 20 dBm was determined. When narrowing the pulse to have constant energy with raising input power a damage occurred in the 1W region.
For integration in high numbers yield and uniformity are important. Due to the etch stop layer the chip performance varies only slightly across the wafer. Figure 4 shows the performance of 55 amplifiers randomly selected from one wafer at a constant drain and gate bias. The RF yield for our tough specification was 56 %.

CONCLUSION

This paper has outlined the requirements, critical design aspects, and excellent electrical performance of a monolithic low noise amplifier for X-band applications. The test results over a great set of LNAs has shown a noise figure of only 1.1 dB and a gain of 19 dB with very high gain flatness over a bandwidth of greater than 30 %. Further critical requirements on high IP3 level, switching behaviour, overload and damage level, temperature behaviour, have been accomplished and demonstrated impressively.

ACKNOWLEDGEMENT

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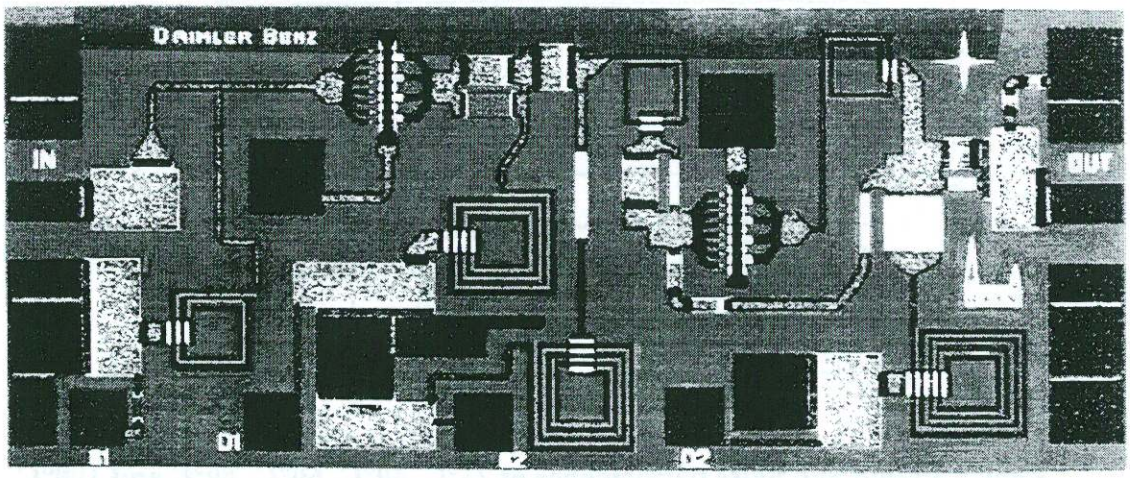

Figure 1: Layout of the LNA chip

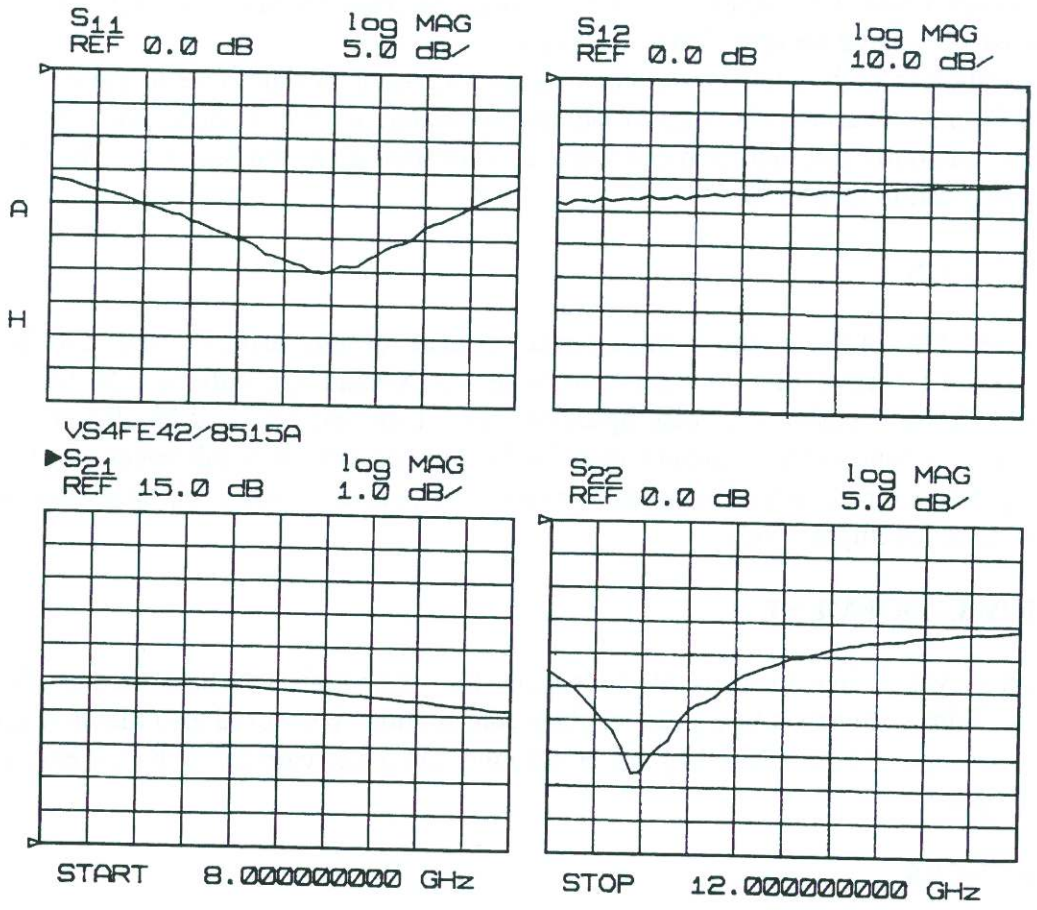

Figure 2: S-Parameters of the LNA at 5V and 50 mA bias

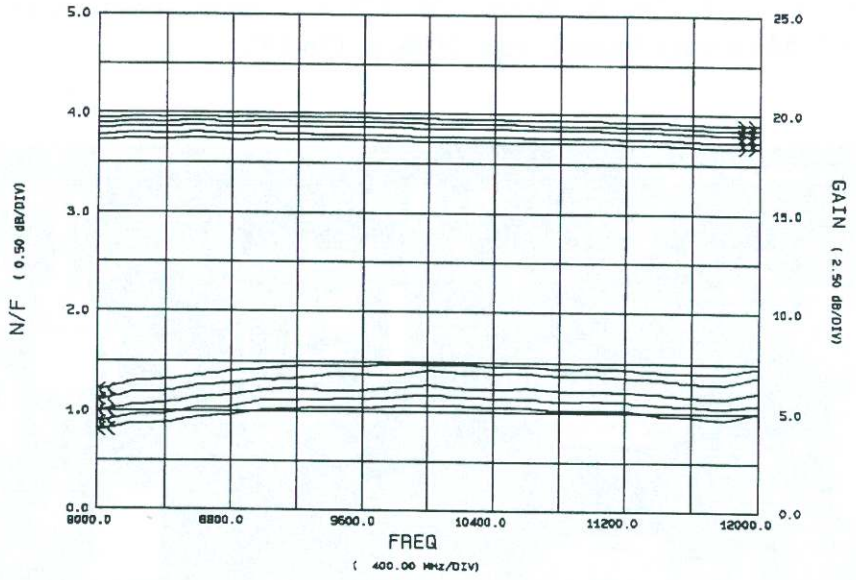

Figure 3:Gain and noise performance at 23°C, 40°C, 60°C, 80°C and 100°C

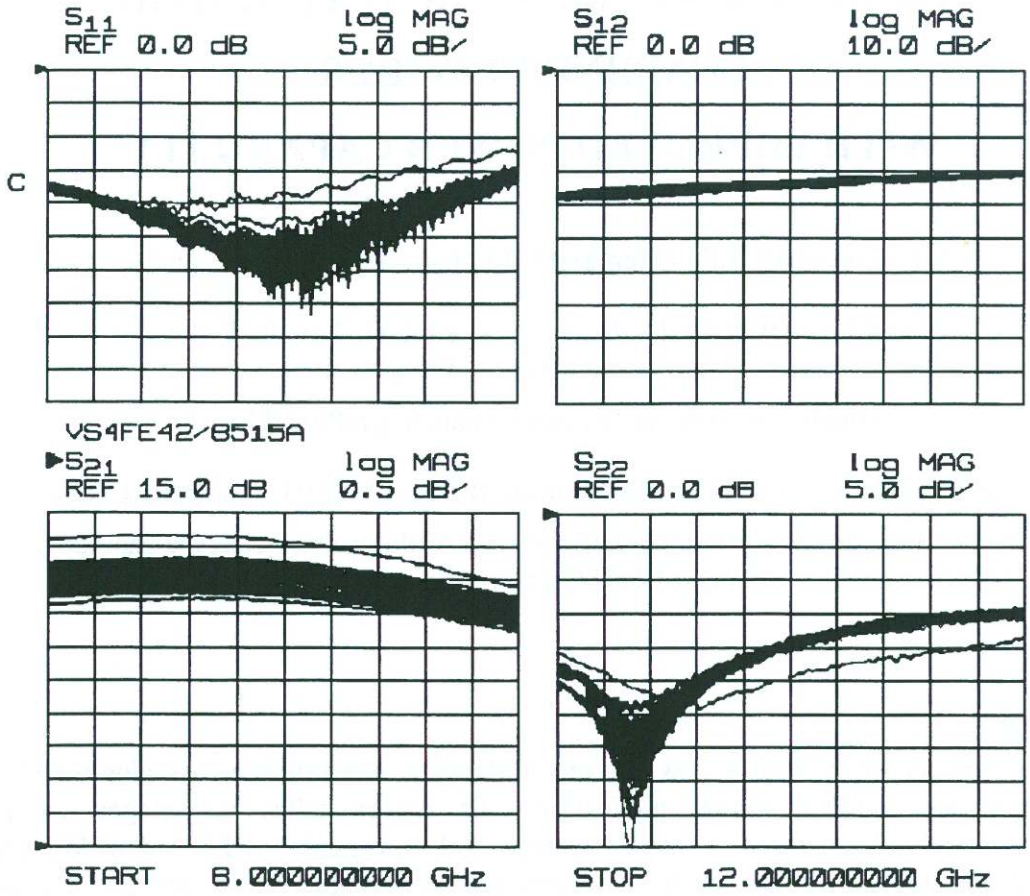

Figure 4: S-Parameters of 55 LNAs at fixed gate and drain voltage randomly selected from one wafer

Frequency Range	8 GHz ... 11.5 GHz
Power Consumption	250 mW (5V, 50 mA)
Small Signal Gain	18.8 dB
Gain Ripple	±0.15 dB
Input Match	≤ -16.5 dB
Output Match	≤ -17.0 dB
Noise Figure	≤ 1.1 dB
1 dB Compression Point	12.5 dBm
Damage Level (10 µS pulse, 10 % Duty Cycle)	≥20 dBm
Switching Time (to ±0.5 dB, pulsed drain)	30 nS
Temperature Dependency of Gain	-0.012 dB/°C
Temperature Dependency of Insertion Phase	+0.01 deg/°C
Temperature Dependency of Noise Figure	+0.008 dB/°C

Table 1: Compilation of measurements results at room temperature