Thermal modeling of GaAs FETs for MMICs CAD with modern design techniques

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Abstract - **In this paper new improved large and small signal thermal models of GaAs FETs are proposed.**

The models are available also in the polynomial form required for thermal CAD of low-power MMICs with low frequency ICs design technique as that based on physical parameters of the foundry.

The aim of the modelling appraoch is to join together large and small signal thermal models, to achieve an efficient CAD technique, and to solve the bias and technology dependence of thermal coefficients.

I. INTRODUCTION

Microwave Monolithic Integrated Circuits (MMICs) applications include the operating temperature from about -50 °C to +120 °C, requiring accurate device thermal models to design. The low thermal conductivity of GaAs makes thermal problems worse [1-3].

Moreover, GaAs monolithic integration allows the implementation of circuit topologies, such as the differential pair and related circuits, up to now used only in low-frequency ICs. This also encourages to GaAs MMICs design, the application of well known low-frequency design techniques, as the one based on physical parameters of the foundry [4]. To this aim each Small Signal Equivalent Circuit Parameter (SSECP) of the device must be in the following analytical form: SSECP = W*P(i) where, in present-day foundry processes, the gate width, W, is the only device parameter open to the circuit designer [4-5] and P(i) is a polynomial function of $i = I_{ds}/I_{dss}$ where I_{ds} and I_{dss} are respectively the drain bias current and the maximum saturation drain current of the device.

Therefore, to satisfy present-day low-power MMICs design requirements it is necessary to simulate thermal effects on the device characteristics by an accurate I-V (current-voltage) modeling [2], an accurate C-V (capacitance-voltage) modeling [6] accounting for FET current and capacitance dependence on temperature, in analytical form useful for MMICs CAD with low frequency design techniques.

Then, the aim of this paper is to propose a new improved small signal thermal model of GaAs MESFETs very accurate in the range of temperature from about -50°C to +120°C. The small signal model is determined directly by the large signal one and is available also in the polynomial form required for thermal CAD of low-power MMICs with low frequency ICs design technique based on physical parameters of the foundry [4].

The approach to define the new model is based on physical considerations about thermal effects, necessary to achieve a reliable design, in spite of its non-physical nature.

II. THE NEW APPROACH FOR SMALL SIGNAL THERMAL MODELING OF GaAs FETs

Classical empirical or semiempirical approaches to develop large signal models of GaAs FETs accounting for thermal effects, are still valid for an efficient CAD of MMICs [2], [6-8]. Nevertheless, analytical calculation of partial derivatives of empirical expressions with respect to bias voltages, in order to obtain small signal parameters, is always a very hard job. In fact empirical expressions must be very bias-dependent if a satisfactory accuracy is to be achieved. On the other hand, numerical calculation of derivatives, and then of the small signal model, does not allow control over design variables to the ICs designer.

On the other hand, physical models must account for the temperature dependence of the major physical factors that influence the GaAs FETs DC and RF parameters: the energy gap, the available state density at the conducting and valence band edge, the dielectric constant, the electron saturated velocity, the electron mobility and the Schottky barrier height [9]. Therefore the approach generally used for the small signal thermal modeling lies in accounting for the temperature dependence of GaAs FET small signal parameters by means of linear or non linear functions of temperature [9]. In these functions temperature coefficients, depending on the technology and bias voltages of the device, appear. This dependence makes device thermal characterization very difficult. Moreover, physical modeling of bias dependence of device characteristics can be accurate enough if analytic expressions account for many device second order effects as the effect of negative device output conductance, especially due to selfheating and substrate currents, backgating, capping, Gunn domain formation and surface states.

Thus model expressions become very complicated making very difficult to derive the analytic small signal model from the large signal one. Then the task remains of tying up large and small signal models and of adequating the model expressions to low frequency design techniques, in the physical approach too.

The approach to modeling, proposed in this paper, satisfies the modern MMIC design and applications requirements.

This approach is sketched in the schematic-diagram DF1 shown in Fig. 1 in which a large signal thermal model (physical, empirical or semi-empirical) is transformed in the polynomial form by means of an adequately developed computer program (first transformation program in DF1) and, subsequently, from the polynomial large signal model it is easly derived the small signal thermal model of the device, by means of a computer program, also (second transformation program in DF1). This means that the polynomial coefficients are calculated from the large signal model by means of a small and quick computer program whose input is the set of the large signal empirical parameters and whose final output is the set of the small signal polynomial coefficients.

In this way the designer does not lose the control over physical and technological device parameters, if the large signal thermal model guarantees it.

Moreover, the polynomial form of the small signal thermal model offers many advantages: it is very quick to implement and to execute in the commercially available circuit simulation programs; it is easy to reduce in the form SSECP = W*P(i) required from the recently proposed MMIC design technique based on physical parameters of the foundry [4] accounting for the simplifier assumptions on which the technique is based; moreover, the polynomial form allows to simulate very easly thermal effects, as it will be shown in the next section.

Hence the problem of the small signal thermal coefficients bias and technology dependence is solved calculating SSECPs directly from the large signal model, thus also binding large and small signal models together. The polynomial degree depends on the particular SSECP considered and its maximum value is three.

The approach is useful for any large signal thermal model that satisfies previous requirements; moreover as an example it is considered in the next section a large signal thermal model developed by the authors [2, 6, 10, 11]. Then, it is developed the small signal thermal model, i. e. the expressions for the transconductance, g_m, for the output conductance, g_{ds}, for the internal resistance R_i and for the gate capacitances, C_{gs} e C_{gd}.

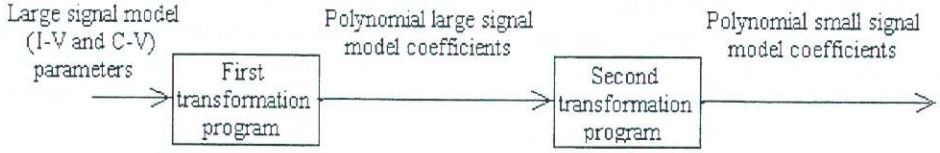

Fig. 1 - Transformation diagram DF1.

III. NEW LARGE AND SMALL SIGNAL THERMAL MODELS OF GaAs FETs

According to the procedure previously described to model the GaAs FET a large signal thermal model of the device is firstly considered, very accurate in the range of operating temperature of interest.

IIIa. Description of the large signal thermal model

The model simulates thermal effects simply by modeling the dependence on temperature of the device threshold voltage, maximum saturation drain current and electron saturated velocity, as suggested by physical considerations about thermal effects.

The proposed large signal I-V model [2], [12] is an empirical one whose most important feature is to simulate very accurately the effect of negative device output conductance, especially due to Gunn effect, selfheating and substrate currents. It simulates external thermal effects, due to operating temperature of FET different from the reference temperature, mainly modeling the dependence on temperature of the device threshold voltage and of the maximum saturation drain current, because of their strong sensitivity to the temperature variations as suggested by a device physical behaviour analysis [2]. The extraction of empirical parameters is facilitated because of the calculation of their initial values by physical expressions.

Details about model expressions, bias and temperature dependent empirical parameters and their extraction procedure are in [2], [10].

The C-V large signal model is a semiempirical one [8], [11]. It accounts for many important microwave effects such as backgating, capping and electron velocity saturation, Gunn domain formation and surface states.

Starting from a physical model of the MESFET gate capacitances, C_{gs} and C_{gd}, it was improved the accuracy introducing the concept of "effective shape of the depletion region", as shown in Fig.2, determined by means of a few empirical parameters that optimize the fitting between measured and modeled capacitance values, compensating physical approximations of the model, and allow to extend the model usefulness to epitaxial and ion implanted FETs.

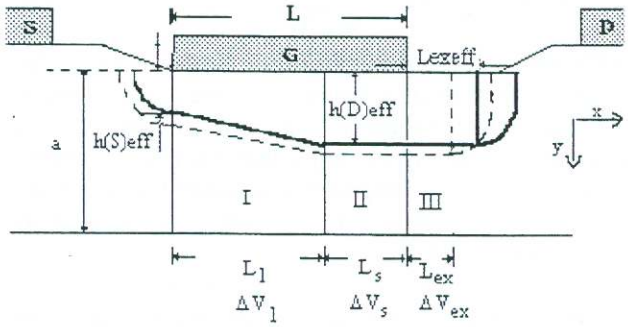

Fig. 2 - The approximated (dashed) and the effective depletion region shape obtained by means of empirical parameters.

These parameters are: the effective thickness of the depletion region at the source and drain edge of the gate, the effective extension of the depletion region in the gate-drain interspace and the effective surface state density variation with the gate voltage. Their physical meaning allows to extract them one at a time very quickly and easly, their initial values being estimated by physical expressions [11].

Details about the C-V model expressions available to reference temperature are in [8] and [11]. They are obtained evaluating the charge in the effective depletion region, accounting for the previous microwave effects, and making derivatives respect to bias voltages.

Moreover, the temperature dependence of capacitances is modeled by linear functions of temperature, as demonstrated in [9], whose coefficients are related to the I-V thermal model and to the electron saturated velocity dependence on temperature [9].

In fact, once the temperature dependence of the threshold voltage (in the I-V model), of the energy gap and of the electron saturated velocity have been determined, it is possible to calculate the temperature dependence of the built-in voltage, of the intrinsic concentration, of the electron mobility and of the dielectric constant. Therefore, the temperature coefficients for C_{gs} and C_{gd} respectively, are determined using simple Schottky junction theory C-V model [12] and they are assumed to be still valid for the authors semiempirical model. Then capacitances as function of temperature are expressed by:

$$C_{gs,d}(V_{gs},V_{ds},T) = C_{gs,d}(V_{gs},V_{ds},To)*[1+C_{th}*(T-To)]$$

where the term $C_{gs,d}(V_{gs},V_{ds},To)$ is calculated by equations of the authors C-V model, useful at reference temperature To. Therefore it is not necessary to make measurements of S parameters at temperatures different to room one to obtain an enough accurate estimation of internal capacitances thermal dependence.

IIIb. Description of the small signal thermal model

In order to calculate the device SSECPs at any temperature the large signal model is transformed in polynomial form. To avoid a great loss in the model accuracy, the polynomial approximation is made in a arbitrarly small neighborough of the bias point of interest. Then, the polynomial large signal I-V model in an arbitrary range of bias voltages becomes as follows:

$$I_{ds}(V_{gs},V_{ds},T) = \sum_{j=0,3} V_{ds}^{\ j} * \left(\sum_{k=0,3} c_{jk} * V_{gs}^{\ k} \right) \qquad (1)$$

Coefficients c_{jk} are the output of the first transformation routine of diagram DF1, whose input are the parameters of the large signal thermal model. Coefficients c_{jk} are automatically calculated at any temperature T of interest. Therefore, they are temperature dependent and can be also expressed by means of interpolation polynomial in the subsequent form:

$$c_{jk} = c_{jk}(1)*T^4 + c_{jk}(2)*T^3 + c_{jk}(3)*T^2 + c_{jk}(4)*T$$

in which polynomial coefficients can be also calculated by means of the first transformation program.

Then, the transconductance g_m and the output conductance g_{ds} are easly calculated deriving polynomials:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = \sum_{j=0,3} V_{ds}^{\ j} * \left(\sum_{k=1,3} k * c_{jk} * V_{gs}^{\ k-1} \right) \qquad (2)$$

$$g_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}} = \sum_{j=1,3} j * V_{ds}^{\ j-1} * \left(\sum_{k=0,3} c_{jk} * V_{gs}^{\ k} \right) \qquad (3)$$

Derivatives, and then the small signal model parameters, are automatically calculated by means of the second transformation program of the diagram DF1.

Similarly, the gate capacitances are expressed as:

$$C_{gs,d} = \sum_{j=0,3} V_{ds}^{\ j} * \left(\sum_{k=0,3} h_{jk} * V_{gs}^{\ k} \right) * [1+C_{th}*(T-To)] \qquad (4)$$

where coefficients h_{jk} are bias and technology dependent, but are independent on temperature and are automatically calculated by the first transformation program of the diagram DF1.

Subsequently, the form SSECP=W*P(i), required to design MMICs with the physical parameters of the foundry technique, can be very simply obtained.

In fact, the considered MMIC design technique involves the following assumptions and approximations:

i) the FET currents are indipendent on V_{ds}. This means that they are fixed by the other circuit elements.

ii) The SSECPs depend only on bias current, I_{ds}, and gate width, W, and are independent on V_{ds}.

Because of the previous assumptions, the design technique requires device SSECPs according to the following expressions [4], [10]:

$$i = f(V_{gs}) = a_1 V_{gs}^{\ 2} + a_2 V_{gs} + a_3 \text{ and then} \qquad (5)$$

$$V_{gs} = f(i) = [\, -a_2 \pm (a_2^{\ 2} - 4a_1*(a_3 - i))^{0.5}]/(2a_1); \qquad (6)$$

$$C_{gs} = W*(\, b_1 V_{gs}^{\ 3} + b_2 V_{gs}^{\ 2} + b_3 V_{gs} + b_4); \qquad (7)$$

$$C_{gd} = W*(\, c_1 V_{gs}^{\ 3} + c_2 V_{gs}^{\ 2} + c_3 V_{gs} + c_4); \qquad (8)$$

$$g_m = dI_{ds}/dV_{gs} = W*J_{dss}*di/dV_{gs} = W*J_{dss}*(2a_1 V_{gs} + a_2) \qquad (9)$$

being V_{gs} given by (6);

$$g_{ds} = dI_{ds}/dV_{ds} = W*J_{dss}*di/dV_{ds}; \qquad (10)$$

$$R_i = v_{sat}*L/(\mu_n*W*J_{dss}*i) \qquad (11)$$

that can be immediately calculated by (1)-(4) considering the saturation current independent on V_{ds}, for all SSECPs except for g_{ds}.

The scalable model in the last form (5)-(11) is determined also automatically by means of the computer program in diagram DF1.

IV. EXPERIMENTAL RESULTS

To confirm the validity and usefulness of the proposed GaAs FET thermal models and to verify their accuracy many MESFETs fabricated by ALCATEL and FUJITSU were d.c. and r.f. characterized in the Tecnopolis-CSATA microelectronic division laboratories and simulated by the new models. The relative error between measured and modeled values of device d.c. and r.f.

parameters was found to be very poor, often less than 1%. This is an excellent result that confirms the improved accuracy of the model.

Fig. 3 shows I/W-V fitting curves in the saturation region at room temperature for a 0.5 μm ion-implanted MESFET (2TX102) while figs. 4-5 show the capability of the large signal model to fit the effect of operating temperature different from the reference one on the I-V curves of the same device.

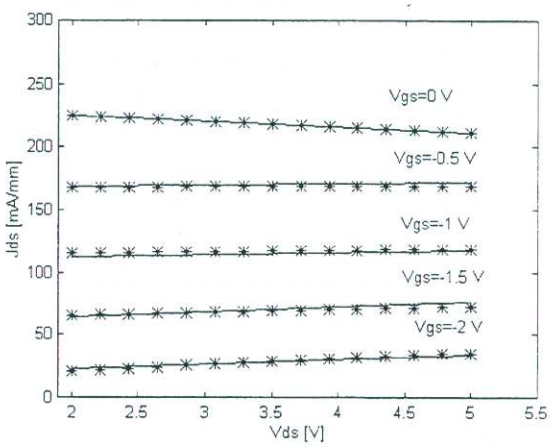

Fig. 3-Modeled (*) and measured, I_{ds}, normalized respect to W.

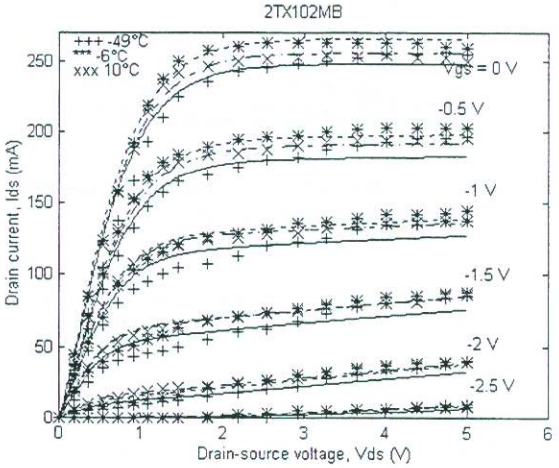

Fig. 4- Measured and modeled I-V curves at -49, -6 and 10 °C

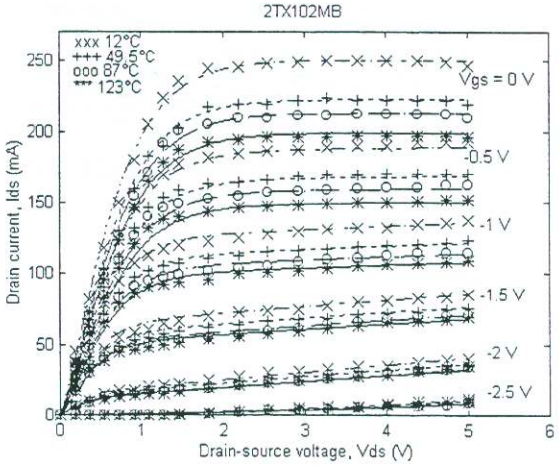

Fig. 5 - I-V curves at 12 °C, 49.5 °C, 87°C, 123°C

Figures 6-7 show the C-V fitting curves at room temperature, 300 K, for 2TX102 device, modeled with the physical (o) and semiempirical (-) model.

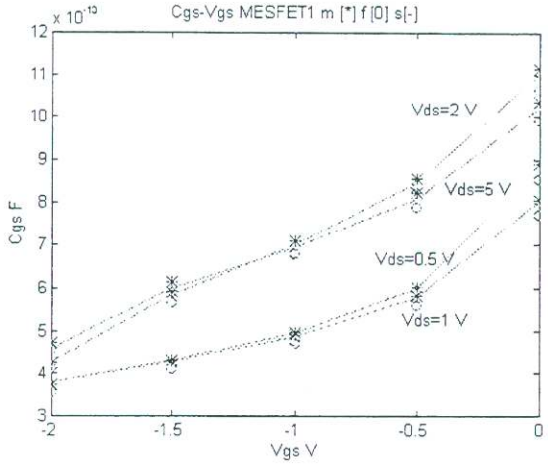

Fig. 6-C_{gs}-V_{gs} fitting curves for 2TX102 device

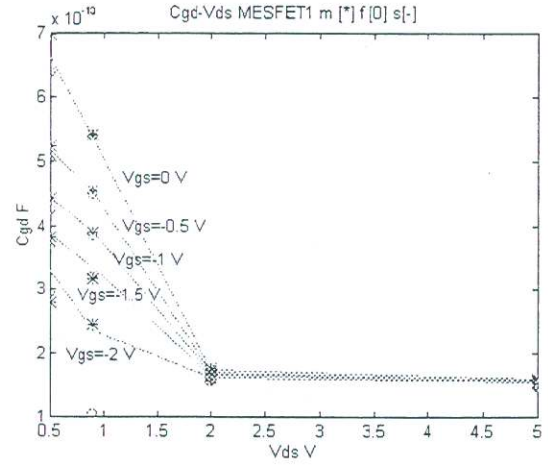

Fig. 7- C_{gd}-V_{ds} fitting curves for 2TX102 device

As show figsures 6 and 7 the introduction of empirical parameters in the C-V physical model improves significantly the model accuracy.

Figures 8-11 show measured (*) and modeled SSECPs of the same FET. The agreement is very satisfactory.

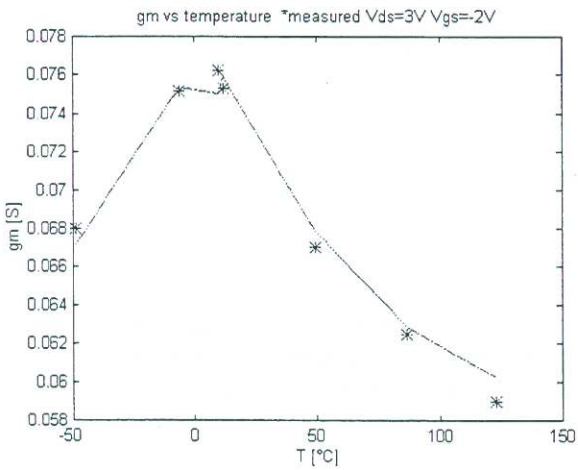

Fig. 8

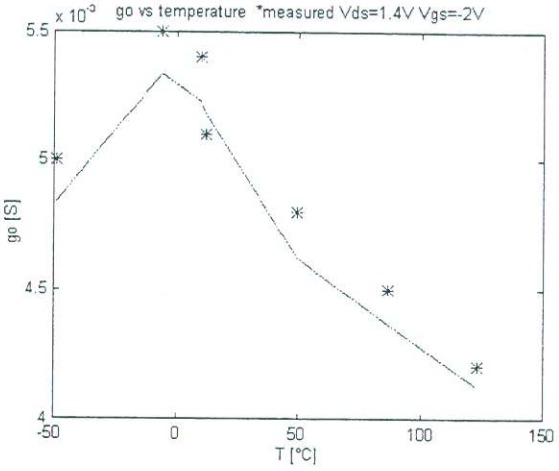

Fig. 9

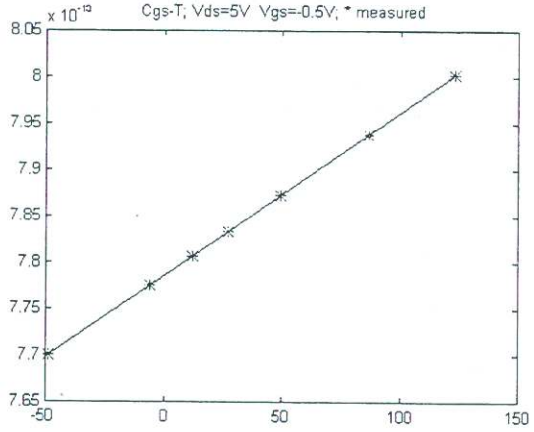

Fig. 10

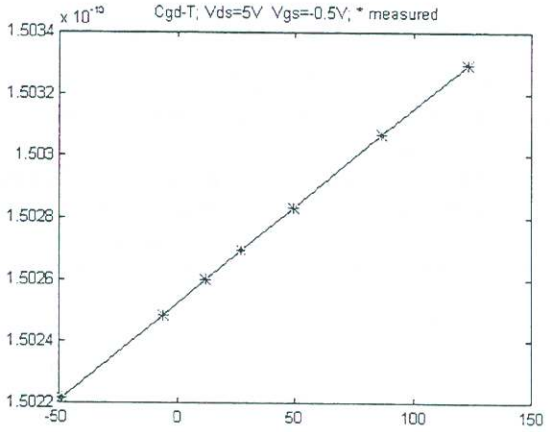

Fig. 11

Figs.8-11: SSECPs (transconductance gm [S], output conductance go [S], gate-source capacitance Cgs [F], gate-drain capacitance Cgd [F], respectively) measured (*) and modeled (-) values vs temperature [°C] for the 2TX102 FET.

Figures 12-16 show the accuracy of the model to simulate other kinds of MESFETs.

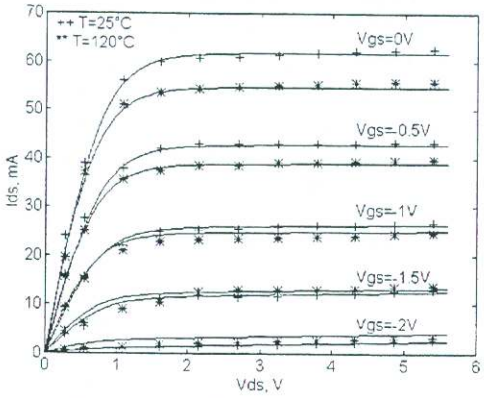

Fig. 12 - I-V fitting curves for another 0.5 μm device

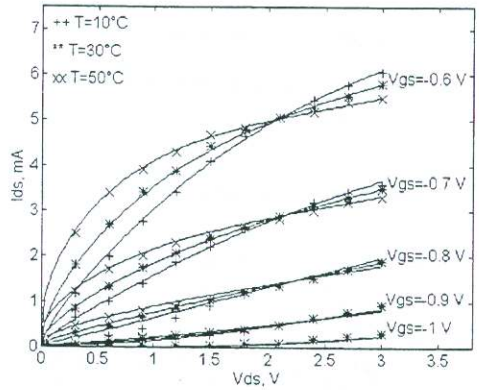

Fig. 13 - I-V fitting curves for a 4 μm MESFET at positive operating temperatures

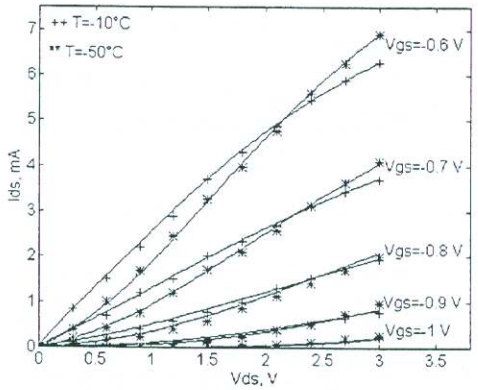

Fig. 14 - I-V fitting curves for the previous 4 μm MESFET at negative operating temperatures

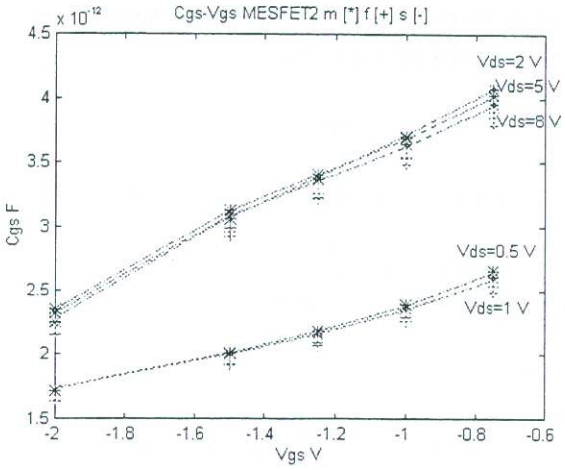

Fig. 15 - C_{gs}-V_{gs} curves for a 1 μm epi MESFET at 27 °C.

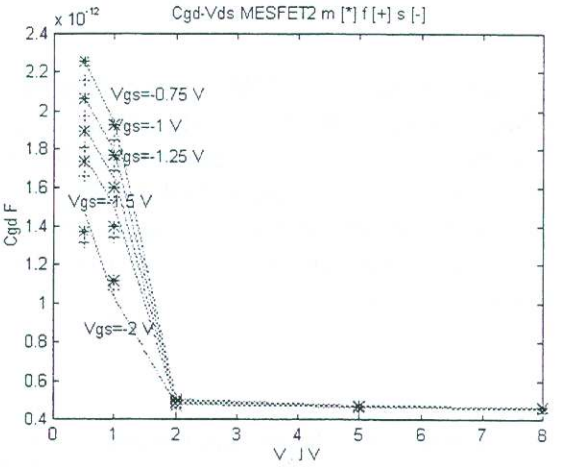

Fig. 16 - C_{gd} -V_{ds} curves for the previous 1 μm epi MESFET at 27 °C.

V. CONCLUSIONS

In this paper improved large and small signal thermal models of GaAs MESFETs have been proposed.

The small signal model was directly determined from the large signal one in polynomial form by means of a computer program, whose input are the empirical parameters of the large signal thermal model, that calculates, at any temperature, the coefficients of the polynomial directly from the large signal model, thus binding large and small signal model together and thus solving the problem of the samll signal thermal coefficients bias and technology dependence.

The small signal model is available also in the form useful for thermal CAD of low-power MMICs with the recently developed low frequency ICs design technique based on physical parameters of the foundry.

The small signal model guarantees a reliable design because it allows to the ICs designer the control over physical and technological device parameters, in spite of its non-physical nature.

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