

Gate lag in InP HFET : influence on digital circuits

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I-Introduction:

The GaAs MESFET is widely used in high speed digital transmission. But the frequency dispersion of both transconductance and output conductance, mainly due to traps, often penalizes the use of these devices in circuit applications (1). In the time domain these parasitic effects lead to a distortion of the transmitted pulse and to the shift of the logic levels. GaAs P-HEMTs are known to exhibit less distortion and gate lag effects. InP HFETs are also susceptible to drain/gate lag effects (2). We report on comparative measurements on GaAs MESFET, GaAs P-HEMT and InP HFET in order to gain a better understanding of the role of traps in InP HFETs.

II- Experimental set up:

a- Description of the three structures:

The commercially available reference GaAs MESFET uses a three-layer epitaxial structure with a recessed $0.3 \mu\text{m}$ gate length. The surface of the device is passivated with SiO_2 and Si_3N_4 double dielectric layer. The GaAs P-HEMT structure has a pseudomorphic $\text{In}_{0.22}\text{Ga}_{0.78}\text{As}$ channel with an undoped $\text{Al}_{0.22}\text{Ga}_{0.78}\text{As}$ barrier layer. The gate length is $0.5 \mu\text{m}$. A Si_3N_4 layer is deposited on the surface to protect the active areas and to prevent the formation of unstable Ga and As oxides at the surface. The third structure is an InP HFET doped channel structure processed in our laboratory (3). The layers are grown on (100) semi-insulating InP(Fe) substrate with InAlAs for buffer and barrier layers and a channel comprising of : 25 nm InP doped channel, 2 nm InP spacer layer, 4 nm InGaAs undoped channel (figure 1). The gate length is $0.8 \mu\text{m}$ and the characteristics exhibit some limited kink effect (2). A SiN layer is deposited on the surface by UV - enhanced Chemical Vapour Deposition (UVCVD) which is a soft process as the energy is provided by UV photons from a low-pressure Hg lamp.

b- Measurements setup:

The inverter amplifier makes possible to check both static and dynamic electrical performances of each type of transistor (1). The circuit consists of the FET under test with its load resistor. A pseudo-random input sequence is applied to the gate and the corresponding pseudo-random output sequence is observed on a 50Ω load resistor. The gate lag set up allows measurements across a 1Ω resistor of drain current transients when the gate is pulsed at constant V_{ds} . When the gate is forward pulsed from pinch-off, the drain current switches partly on, then lags with a time constant in the $0.1 - 1 \text{ ms}$ range for the MESFET.

III- Results and Analysis:

The difference in logic level shift behaviours between GaAs MESFETs and GaAs P-HEMTs or InP HFETs is strongly related to their gate lag behaviours, as reported below.

a- Results:

To increase the observed drift in logic levels, a low bit rate pseudo-random sequence is applied to the gate of each transistor. A shift of the logic levels is only observed for the MESFET structure. On figure 2 a, a shift of logic levels "0" and "1" is shown, that will reduce the eye pattern opening. Whatever the bit rate, no such effect is observed with InP HFET or GaAs P-HEMT (fig. 2 b & c). This shift is associated to drain lag/gate lag. In the voltage gain formula (1), and provided the load resistor is small enough (i. e. 50Ω), the impact of the drain lag, associated to g_d , is less important than the gate lag associated to g_m .

$$A(f) = \frac{-g_m(f)}{g_d(f) + \frac{1}{R_L}} \quad (1)$$

Even if the three transistors exhibit observable and similar drain lag, its effect on the pseudo-random pulse pattern is not significant. It is not the same for the gate lag. The differences in gate lag reflect the difference in structure (fig. 3).

b- Analysis: Rocchi's model

The model by Rocchi (6) is used to explain the gate lag of any FET: the surface traps are at the origin of the source access resistance change and of the transconductance frequency dispersion. The channel carriers get trapped by the surface traps. It leads to the modification of the band bending with, as consequence, the change of the gate-source access resistance. For instance the transconductance is smaller at high frequency than at DC if the gate-source access resistance increases in time.

$$g_m = \frac{g_m^*}{1 + R_s \cdot g_m^*} \quad (2)$$

The gate lag effect is thus associated to the time dependence of the gate-source access resistance R_s (2). Right after the pulse is applied to the gate, the channel right under the gate opens up, but not the gate-source access region which relaxes with a slow time constant. In GaAs MESFETs, the gate lag can be important. In GaAs P-HEMTs, the gate lag is quite small because of the barrier-channel discontinuity, and dependent on the position of the doped barrier region. In InP HFETs, the gate lag is negligible because of the undoped barrier and because of its large band gap material (large barrier-channel discontinuity for electrons).

The shift in logic levels is thus associated to traps located at the surface between gate and source and to the associated gate lag. Gate lag and drain lag effects are superimposed in the voltage response but the effect of drain lag is very small compared to the effect of gate lag as mentioned before. This gate lag is present on GaAs MESFET and not on P-HEMT or InP HFET (figure 3). The reason is that in a MESFET the surface traps are accessible to channel carriers (4). In the P-HEMT or in the InP HFET, the barrier layer reduces significantly the carrier flow between surface traps and channel (5).

Even if the surface treatment does not modify the trap density, it stabilizes the surface. The insulator layer avoids surface interaction with the atmosphere and contributes to prevent the loss of channel

carriers. Consequently surface passivation cannot be neglected for devices such as MESFET and PHEMT whose structures are more sensitive to surface effect.

IV- Conclusion:

We have observed parasitic effects due to electron traps located at the surface close to the gate and at the interface channel-buffer and channel-barrier interfaces. A different behavior for GaAs MESFETs compared to GaAs PHEMTs or InP HFETs is observed. The GaAs PHEMT and the InP HFET do not present severe problems connected to traps at low frequency.

V- Acknowledgements:

The author would like to thank G. Post, J. Décobert, C. Courbet, who have participated in the design and in the fabrication of the devices.

VI- References :

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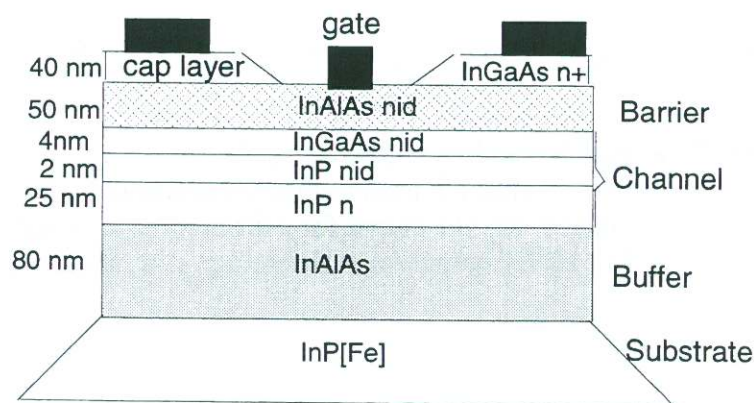


fig. 1 : A cross sectional view of the InP HFET.

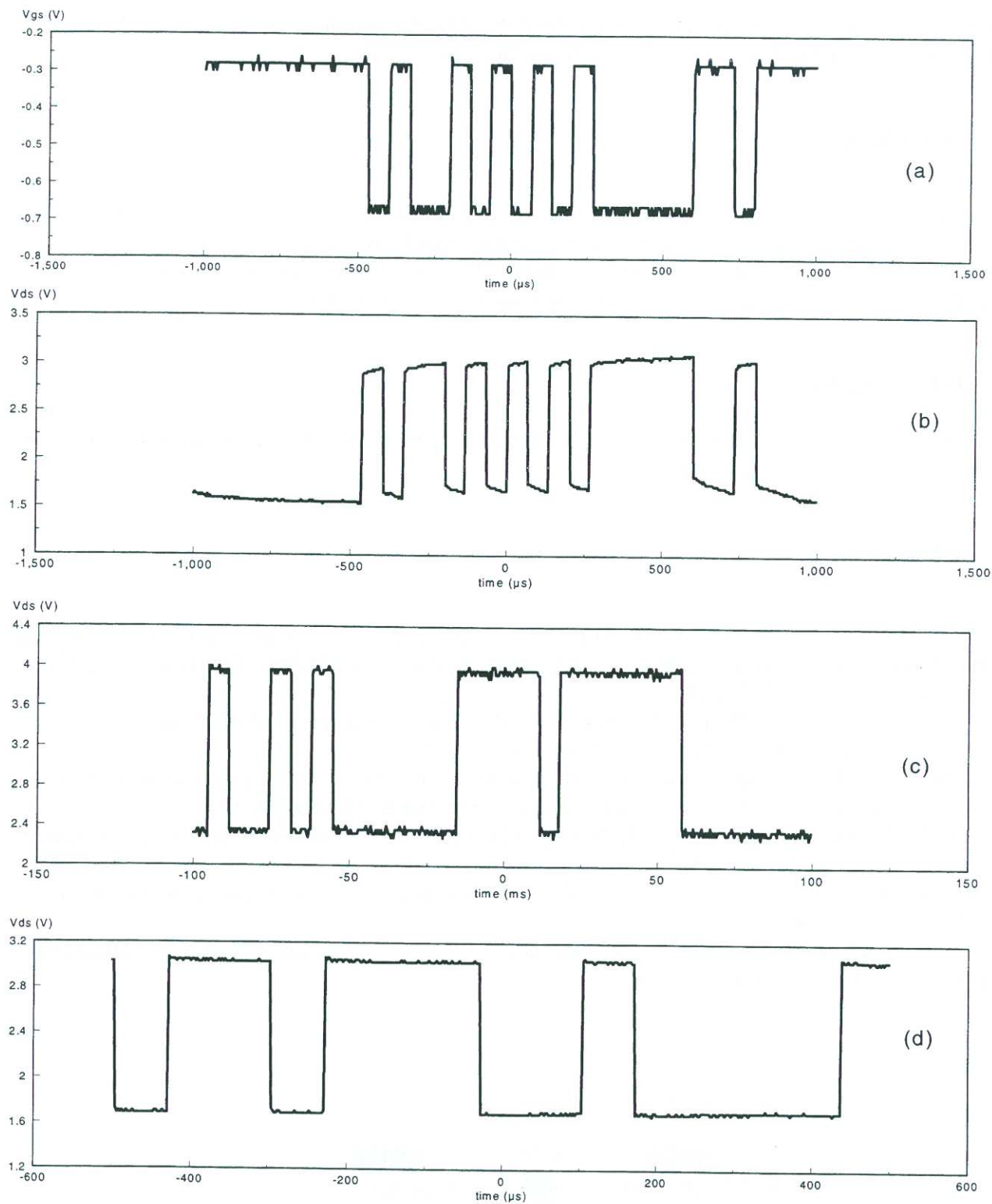


fig. 2 : a- pseudo-random sequence input
 b- GaAs MESFET pseudo-random sequence output
 c- GaAs P-HEMT output for a different p. s. -r. sequence input
 d- InP HFET output for a different p. s. -r. sequence input

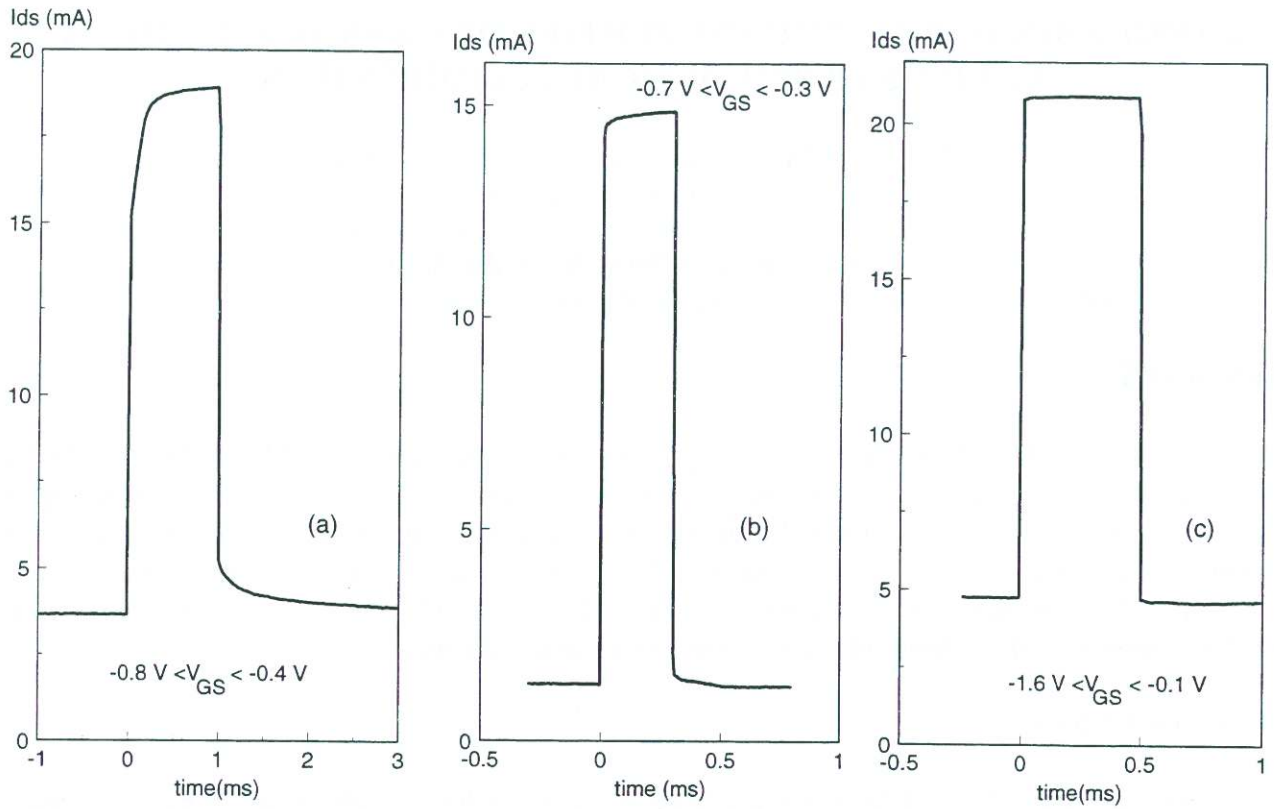


fig. 3 : Gate Lag Outputs at $V_{ds} = 3 \text{ V}$
 a- GaAs MESFET b- GaAs P-HEMT c- InP HFET