POSITIVE FEEDBACK GaAs COMPARATORS FOR SDH/SONET APPLICATIONS

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ABSTRACT

In this paper we present two topologies for differential high-sensitivity comparators, suitable to be implemented in GaAs MESFET/HEMT technologies. Both topologies use positive feedback to compensate for the moderate specific transconductance of GaAs devices, and differ for the implementation of the summation node. The linear and non-linear behaviour of the circuits are analysed, in order to define limitations due to process parametric dispersion using state of art technologies. Circuit simulations are reported to estimate slew rate performance. The topology based on the cascade of two differential cells shows better slew rate performance and results not very sensitive to process parameter dispersion, whereas the topology based on the shunt connection of two differential pairs is more sensitive to process variations but allows to electronically control its DC transfer function.

INTRODUCTION

Optical multigigabits-per-second transmission systems require a non-linear element to provide the proper signal level to the clock and data recovery circuit (CDR), regardless of the input optical power, that can vary over a 20 dB range [Buchwald and Martin (1)]. A possible solution is the use of a comparator, that reshapes the data signal, yielding sharp transitions and saturated output levels, so minimising the effect of noise on the following stages and reopening the eye diagram before the CDR circuit. The comparator acts as an analog to digital interface, with an input sensitivity of a few tens of mV, in order to reduce the influence of jitter on the clock recover circuit performance. The use of a quasi-linear comparator in digital channel is advisable to minimise jitter due to amplitude-to-phase conversion caused by additive noise. The solution preferred is a comparator with very small input dynamic range (then large gain) and without hysteresis loop. Moreover, in the DC-coupled wide bandwidth amplifying chains, the use of differential topologies is advisable, due to the need of controlled output dynamic ranges, to their low sensitivity to common mode signals and to their capability to symmetrise the eye diagram of the output signal [Rein & Möller (2)].
GaAs FET technologies remain the preferred choice for systems operating in the multigigabits-per-second data-rate range, but the moderate specific transconductance of FET devices (about 500 mS/mm typical) [Haigh & Everard (3), Golio (4), Ross et al. (5)] makes difficult to design comparators conforming to the previous requirements. The CDR circuit requires an input signal with an amplitude of some hundred mV to allow the full switching of the digital circuits it includes. The simple differential pair is not adequate to be used as comparator, since it would need an input signal of some hundred mV to yield saturated outputs of adequate amplitude. Therefore proper topologies have to be found to meet specifications on rise/fall times and sensitivity.

POSITIVE FEEDBACK TOPOLOGIES

In this paper we propose two circuit topologies for a GaAs FET comparator, based on a double differential pair: one differential cell (named IDP, input differential pair) is fed by the input signal, and the other (FDP, feedback differential pair) is fed by the output signal with a phase chosen to achieve positive feedback and to increase the DC sensitivity. The topologies presented are based on the block scheme shown in Figure 1: the summation element and the voltage buffer form a positive feedback loop on the differential signals, and the topologies differ in the implementation of the summation node.
The summation node can be represented by the following equation (all voltages are to be intended as differential):

$$V'o = \alpha * Vo = \alpha * (a * V_{i1} + b * V_{i2}) \tag{1}$$

where the term α is the voltage gain of the buffer stage, Vi1 = Vi and Vi2 = V'o. The input-output AC transfer function of the comparator is then given by:

$$\frac{V'o}{Vi} = \frac{a\alpha}{1 - \alpha b} \tag{2}$$

In principle the use of positive feedback can increase the DC gain of an amplifier stage up to the desired level, but the transfer function can become very sensitive to process variations. The robustness of the design can be evaluated by considering the sensitivities of the parameters a, b, α, which define the I/O transfer function of the circuit, with respect

to process parametric dispersion. The use of positive feedback allows both circuit topologies to show a linear or bistable behaviour, depending on the amount of feedback.
In the next paragraphs both circuit topologies are analysed, taking into account the effect of process parametric dispersion, and their simulated behaviour is presented. Simulations have been performed using device models from IAF DPD-QW GaAs technology [Köhler et al. (6), IAF (7)], that makes available enhancement and depletion type 0.3 μm HEMT's.

SHUNT SUMMATION NODE TOPOLOGY

The first topology we present is based on the shunt summation node (SHN) shown in Figure 2. The linear behaviour of the circuit is quite clear: the output currents of the two differential pairs are added in the load resistors R_L, therefore the parameters a and b in (1) are given by:

$$a_{SHN} = g_{mI} R_L \tag{3.a}$$

$$b_{SHN} = g_{mF} R_L \tag{3.b}$$

where g_{mI} and g_{mF} refer to FET's in the IDP and FDP respectively. The small signal gain V'o/Vi can be controlled by varying the input common mode level V_{IDC} (DC bias of IDP) and so changing the ratio of the currents driven by IDP and FDP; the decrease of the input common mode level of the IDP below a certain value leads to the appearance of an hysteresis loop. This happens when the condition set by equation (4) is met:

$$V_{FDC} - V_{IDC} + \frac{Ig * R_L}{2} \geq \Delta(ZI, ZF) \tag{4}$$

where V_{FDC} is the input bias voltage of the FDP and Δ(ZI, ZF) is the input voltage dynamic range of the differential cell formed by one FET of the IDP and another one of the FDP. It can be seen that

$$\Delta(ZI, ZF) = Vgs_F(Ig) - Vt \tag{5}$$

where $Vgs_F(Ig)$ is the gate-source voltage of the FET in the FDP for a channel current Ig, and Vt is the threshold voltage of the FET's in the IDP. In this condition the active FET of the FDP sinks the whole current Ig, driving under cut-off both FET's of the IDP. Therefore the input signal has to change its polarity before the off FET in the IDP turns on, reducing the current carried by the active FET of the FDP and so forcing the output voltage to switch polarity. Figure 3 shows the DC transfer function of the circuit versus the input bias voltage V_{IDC} of the IDP, using the circuit parameters shown in Table 1: small variations in the input bias voltage V_{IDC} result in a different behaviour of the comparator (linear instead of bistable) or in changes of the width of the hysteresis window. This topology therefore results very sensitive to process parametric dispersion, since a variation of the output common mode voltage of the preceding DC-coupled stage, due to the spread of process parameters, seriously affects the DC transfer function, even modifying the circuit behaviour. In our opinion it results appropriate for stable GaAs technologies (e.g. MESFET's with gate length above 0.5 μm) or when input DC-coupling is not required; in such cases the input bias voltage can be used as an active control of AC and DC characteristics.

SERIES SUMMATION NODE TOPOLOGY

The second topology is based on the series summation node (SEN) shown in Figure 4. The parameters defined in equation (1) are obtained as:

$$a_{SEN} = \frac{g_{mu} g_{md} Rx R_L}{2 + g_{mu} Rx} \tag{6.a}$$

$$b_{SEN} = \frac{2 g_{mu} R_L}{2 + g_{mu} Rx} \tag{6.b}$$

where g_{mu} and g_{md} refer to FET's in the up (FDP) and down (IDP) differential pairs respectively.
The comparator based on this topology shows an hysteresis loop if the condition set by equation (7) is met:

$$\frac{Rx * Ig}{2} - R_L Ig + Vgs_F(Ig) \leq Vt \tag{7}$$

where Vt is the threshold voltage of the FET's of the FDP. Equation (7) means that the off transistor in the FDP is still under cut-off when the input signal changes its polarity (FET's in the IDP sinks the same current), and this results in a

bistable behaviour. Equations (6) and (7) show that it is possible to control the DC transfer function in the design phase by choosing an appropriate value for resistor Rx and so selecting between linear and bistable behaviour. Figure 5 shows the DC transfer function of the circuit for different values of the resistor Rx, with the circuit parameters shown in Table 1 and V_{IDC} = -3 V. The DC transfer function is sensitive to the value of Rx, but if such resistor is chosen not too close to the critical value, the circuit behaviour remains as desired (linear or bistable) even for large process parameter variations. Figure 6 shows the DC transfer function versus the input bias voltage, using the circuit parameters in Table 1 and an Rx of 700 Ω (linear behaviour). The series connection of IDP and FDP makes this topology less sensitive to input bias variations, therefore the circuit is advisable also for advanced short channel technologies (e.g. HEMT devices with gate length below or equal to 0.3 μm).

COMPARISON

The main feature of the comparator is the rise time, which describes the capability of handling fast pulsed signals. A useful description of the performance of the circuit is the dependence of the rise time on the input signal amplitude. Computer simulations have been performed to evaluate the performance of the proposed topologies and to make comparison with a simple differential pair. Figure 7 shows the DC transfer function of a differential pair with the same aspect ratio as the proposed topologies (W_D = 30 μm, W_G = 15 μm), that shows a much larger input dynamic range (400 mVpp s.e.). Tables 2 and 3 show rise times for the SHN and SEN topologies respectively, for different input rise times (50, 100 and 150 ps) and amplitudes (1, 2 and 4 times the sensitivity), using the circuit parameters in Table 4 (linear behaviour). The SEN topology shows better slew rate performance, for an input amplitude greater than two times the sensitivity.
A comparator based on the series summation node topology, which achieve the best performance and tolerance to process parameters variations, has been designed using IAF technology: Figure 8 shows the schematic of the circuit, composed of a gain stage (17.5 dB) and the comparator. The circuit uses a single supply voltage of –4.5 V and presents a decoupled input and an open drain output. The output is loaded by 200 Ω resistors and drives decoupled 50 Ω loads. The circuit has been designed to achieve an input dynamic range of 20 mVpp s.e. with a loaded output dynamic range of 800 mVpp s.e. (1.2 Vpp s.e. internal swing), so obtaining rise times below 150 ps. Figures 9 and 10 show the overall DC transfer function and the output eye diagram for a sinusoidal input with 100 mV peak amplitude. Measurement on the fabricated chip are currently carried out in our labs.

CONCLUSIONS

In this paper we have presented two novel topologies for high-sensitivity differential comparators, that use a positive feedback to compensate for the moderate specific transconductance of GaAs devices. Both circuit topologies can show a linear or bistable behaviour, and allow to select the desired shape of the DC transfer function by choosing the appropriate value for a single circuit parameter. The linear and non-linear behaviour of the proposed topologies have been analysed and computer simulations have been performed to evaluate slew rate performance. The shunt summation node topology results more sensitive to process parametric dispersion and input bias voltage, so it is best suited to stable technologies (e.g. GaAs MESFET with gate length above 0.5 μm) or non-DC coupled applications. Anyway it offers the possibility of electrically controlling the DC transfer function by varying the input bias voltage. The series summation node topology is less sensitive to process parametric dispersion, resulting suitable also for less stable, advanced short-channel technologies, and shows better timing performance. A comparator featuring such topology has been designed and fabricated using IAF DPD-QW 0.3 μm GaAs HEMT's technology: simulations show an input sensitivity of 20 mVpp s.e. and rise times below 100 ps.

REFERENCES

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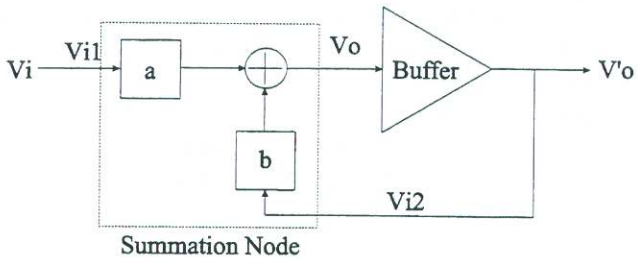


Figure 1: - Block scheme of positive feedback comparators.

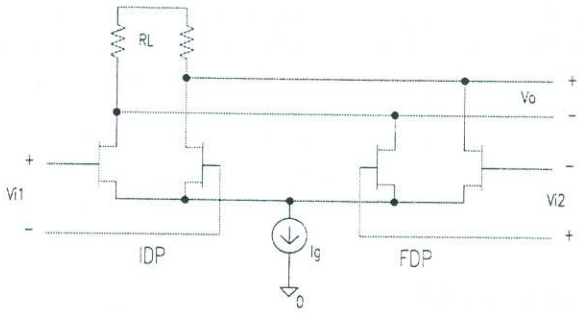


Figure 2: - Shunt summation node.

Table 1: - Parameters for DC simulations.

Comparator core.

R_L	450 Ω
W_I, W_F	30 µm
W_G	15 µm
Vss	-4.5 V

Buffer

W_B	35 µm
W_D (diode connected)	25 µm
W_{GB}	10 µm

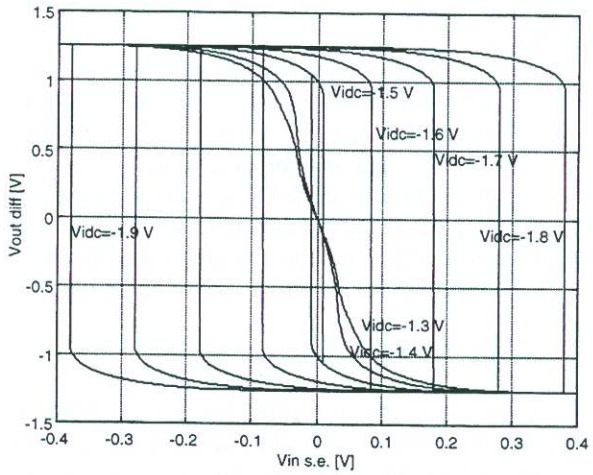


Figure 3: - DC transfer function of the SHN.

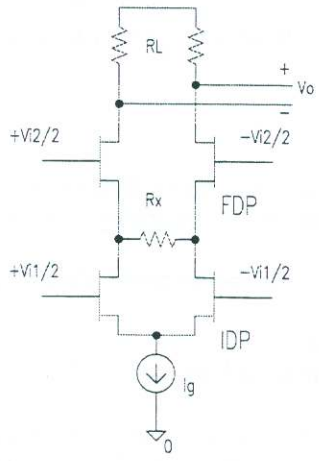


Figure 4: - Series summation node.

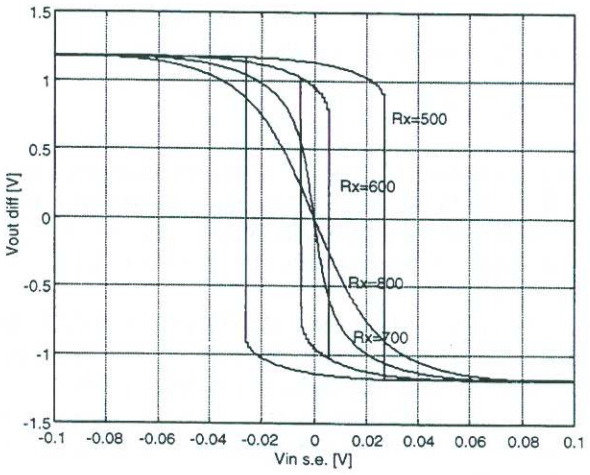


Figure 5: - DC transfer function of the SEN.

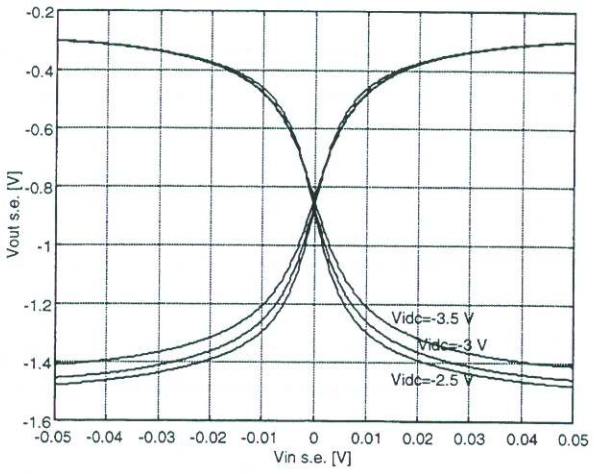


Figure 6: - DC transfer function of the SEN; Rx = 700 Ω.

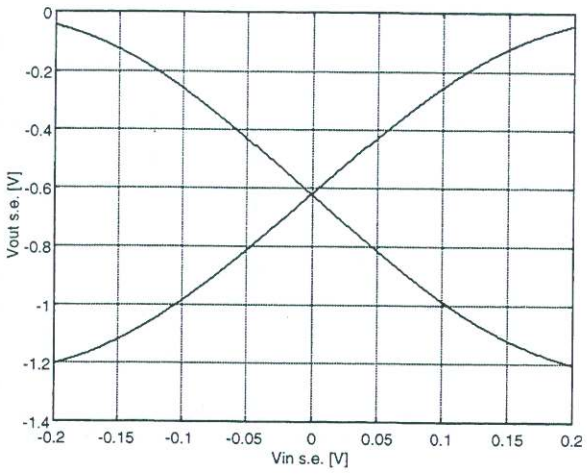


Figure 7: - DC transfer function of a differential pair.

Table 2: - Slew rate performance of the SHN topology.

Input rise time	Vamp / Vsens (Vsens = 150 mVpp s.e.)		
	1	2	4
50 ps	102.2 ps	59.8 ps	62.3 ps
100 ps	110.4 ps	70 ps	62.4 ps
150 ps	124.6 ps	82.4 ps	63.6 ps

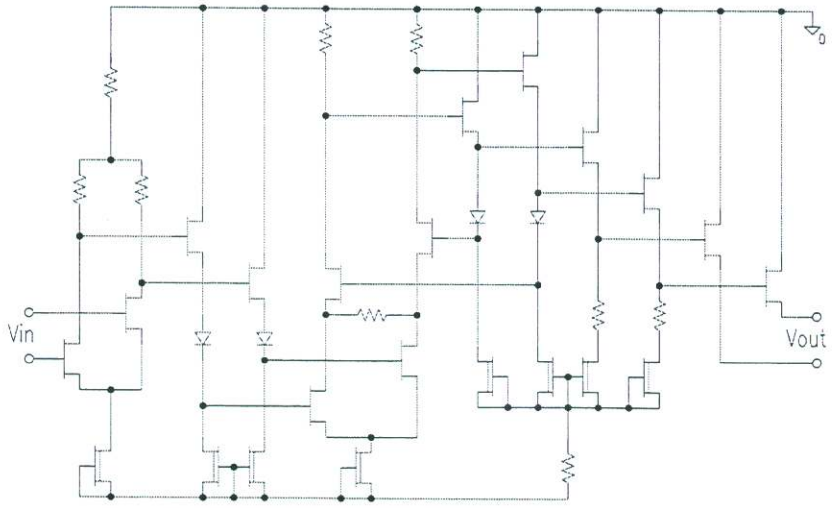
Table 3: - Slew rate performance of the SEN topology.

Input rise time	Vamp / Vsens (Vsens = 70 mVpp s.e.)		
	1	2	4
50 ps	125.4 ps	64.5 ps	35.6 ps
100 ps	130.4 ps	70.9 ps	42.1 ps
150 ps	140.5 ps	81.2 ps	50.7 ps

Table 4: - Parameters for transient simulations.

Comparator core	
R_L	450 Ω
W_I, W_F	30 µm
W_G	15 µm
Vss	-4.5 V
Buffer	
W_B	35 µm
W_D (diode connected)	25 µm
W_{GB}	10 µm
SHN topology	
V_{IDC}	-1.4 V
SEN topology	
Rx	700 Ω
V_{IDC}	-3 V

Figure 8: - Schematic of the comparator.



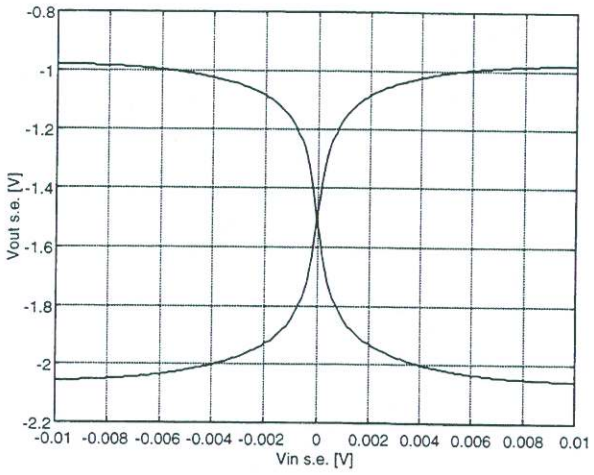


Figure 9: - Overall DC transfer function of the comparator.

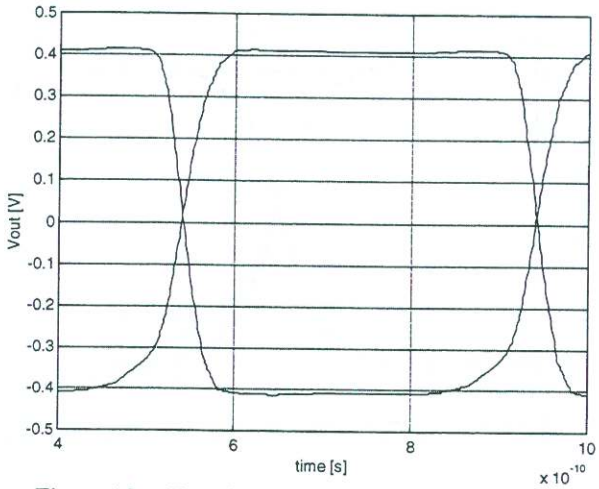


Figure 10: - Transient response of the comparator.

Table 5: - Slew rate performance of the comparator.

Input rise time	Vamp / Vsens (Vsens = 20 mVpp s.e.)			
	1	2	4	10 (typical)
50 ps	91.2 ps	60.7 ps	48.7 ps	43.5 ps
100 ps	94.5 ps	64.8 ps	54.4 ps	44.8 ps
150 ps	100.3 ps	70.6 ps	55.4 ps	50.5 ps