Accurate new scaling routines for any table/function based FET model including temperature and noise behaviour

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ABSTRACT

In this paper we present new scaling routines for any table/function based nonlinear FET model. These measurement based routines are very accurate and can also be used to calculate temperature behaviour. Also the prediction of noise behaviour is possible for scaled devices.

INTRODUCTION

In the last few years many papers have been published concentrating either on noise or on temperature simulation [1] or on scaling routines for special effects like dispersion of the trans- and output conductance of a FET [2]. Our TOPAS (TransistOr PArameter Scaleable) called model is based on an accurate 2D spline table based model [3,4], which combines all the above counted effects within one model. The model has been expanded using two dimensional mathematical functions for describing the intrinsic nonlinear elements. Usually, simple scaling instructions (multiplication or division by 2) are used for scaling a device with the number of gatefingers N or the gatefinger width W_t. Our model uses new and accurate, measurement based scaling routines for all equivalent circuit elements. Furthermore, the same scaling functions can be used for describing the temperature behaviour of the model. The functions are also compatible with the noise simulation and can easily be implemented within every other nonlinear model. To our knowledge this is the first publication on overall scaleable table based models.

EXTRINSIC SCALING PROCEDURE

The fact, that elements of a FET equivalent circuit scale with a factor of 2 (respectively 1/2) can not always be found, as shown in Figure 1 and Figure 2 for different extracted 0.25 µm HEMT devices of the same technology. Some resistances are shown as 1/R to get a scaling function proportional to N and W_t.
While the extrinsic resistances scale by a factor of approx. 1/2, the inductances except L_S remain nearly constant. In our model, which has been implemented into HP-EEsofs series IV (libra), the scaling of the extrinsic elements was taken into account by using a linear expression for S(N) as well as for S(W), e.g.:

$$S_E(N) = a_{EN} \cdot N + b_{EN} \tag{1}$$

The constant coefficients a and b can be found by calculating a linear regression [5]. The whole extrinsic scaling function S_E is described as:

$$S_E(N,W) = S_E(N) \cdot S_E(W) \tag{2}$$

This function delivers even intermediate values useable e.g. for optimization purpose.

INTRINSIC SCALING PROCEDURE

One main requirement for scaling the FETs intrinsic elements is the fact, that the intrinsic elements grids do not change their shapes when changing the device size (Figure 3 and Figure 4). Just the absolute values may change so that one element grid can be calculated from another by multiplying the first grid with a constant number c:

$$c = \frac{\sum_{V_{gs},V_{ds}} \frac{G_x\left(V_{gs},V_{ds}\right)}{G_{ref}\left(V_{gs},V_{ds}\right)}}{n_{Vgs,Vds}}, \tag{3}$$

whereby G_{ref} is a reference grid (the reference scaling factor is 1), G_x the scaled element grid and n the number of bias points taken into account. If the grids G_{ref} and G_x have been extracted for different bias points, they must be spline-interpolated to get the same reference of bias points. The second grid (Figure 4) can be calculated from the first grid (fig. 3) by a multiplication with c = 2.89. This value differs just a little from the usually calculated one

$$c_{old} = \frac{8x75\mu m}{4x50\mu m} = 3 \tag{4}$$

but is more accurate concerning the real device. All scaling values of the intrinsic elements for the examined HEMT devices can be seen in fig. 5 and 6. Most elements show an expected scaling behaviour except R_i, which is due to the fact, that R_i is one of the most frequency dependent elements and small variations of R_G and R_S may cause large variations of R_i during extraction process. Due to the constant grid shape the intrinsic scaling function $S_I(N,W)$ can be calculated by superimposing both single scalings:

$$S_I(N,W) = S_I(N) \cdot S_I(W). \tag{5}$$

A test with the above mentioned c for scaling C_{gs} results in

$$\begin{aligned} c_{new} &= S_I(N = 4 \rightarrow N = 8) \\ &\cdot S_I(W = 50 \rightarrow W = 75) \\ &1.93 \cdot 1.49 = 2.88 \end{aligned} \tag{6}$$

In our model again a linear expression is used to get the intrinsic elements scaling functions, e. g.

$$S_I(W) = a_{IW} \cdot W + b_{IW}. \tag{7}$$

It must be pointed out, that a scaling value of 2.88 only means an error of 4% concerning a value of 3.0. But in worst case all scaling errors may sum up, so that one gets a much larger overall scaling error when using simple scaling factors.

TEMPERATURE DEPENDENCE

For temperature calculations the same proposed scaling functions can be used. Now not different device sizes are scaled but $I_{ds}(V_{gs},V_{ds})$ of the same device at different temperatures. The maximum error that occurs, when scaling e. g. a I_{ds} grid from the reference temperature T = 293 K to T = 253 K using eq. 3, is less then 5% in the ohmic region and less then 1% in the saturation region. All scaling factors for scaling $1/I_{ds}$ with temperature can be seen as dots in Figure 7.

The temperature behaviour including saturation effects (Figure 7) is modeled using eq. 8. Temperature dependence of the intrinsic R_i is been taken care of using eq. 9. As some measurements have shown, the temperature dependence of the capacitances can be neglected.

$$S_{1/I_{DS}}(T) = \begin{cases} a_{1T} \cdot T + b_{1T} & for\, T < T_2 \\ a_{2T} \cdot T + b_{2T} & for\, T_1 \le T < T_2 \\ a_{3T} \cdot T + b_{3T} & for\, T \ge T_2 \end{cases} \tag{8}$$

$$R_i(T) = R_i\left(T_0\right) \cdot \left[\gamma_{Ri}\left(T - T_0\right) + 1\right] \tag{9}$$

NOISE CALCULATIONS

For noise calculation adapted [6] noise equations are used. For a conductance of a noise resistance equation (10)

$$g_R = \frac{\langle i_{th}^2 \rangle}{4kT_0\Delta f} \cdot \frac{T_{sim}}{T_0} \tag{10}$$

is used. The channel noise is modeled using equation (11)

$$g_{Ids} = \left(\frac{1}{4kT_0} k_f \frac{I_{ds}^{a_f}}{f^b} + \frac{2}{3} \frac{T_0}{T_{sim}} \frac{\partial I_{ds}}{\partial V_{gs}} \right) \cdot \frac{T_{sim}}{T_0} \tag{11}$$

T_{sim} is the temperature, for which the noise parameter should be calculated. T_0 is the actual temperature, k_f and a_f are noise coefficients and b is the frequency exponent.

COMPARISON OF THE SCALED MODEL

In this section verification for the scaled model in comparison with small signal S-parameter, noise and temperature measurements on unscaled devices is done to demonstrate the new scaling facilities of our model. Furthermore, an oscillator [7] is simulated temperature dependent.
The results of scaling a 4x50 µm reference device up to a 8x75 µm HEMT are shown in Figure 8 for a bias point of V_{gs} = 0 V and V_{ds} = 2 V. All other comparisons (up- and down-scaled) show the same excellent results for a huge range of bias pints. In fig. 9 the measured s_{21} of a 4x40 µm HEMT at T = 373 K is compared with the simulated
one, scaled again from the reference device at T = 279 K. Although for the scaled model only the gatefinger width is reduced by 20%, it can be seen, that our scaling functions are much more accurate then the simple scaling procedure. Fig. 10 shows the minimum noise figure NF_{min} simulated with the same model, but scaled down to a 40 µm device.
All simulations show perfect agreement with measurements.
Figure 11 shows the frequency and the power of the output signal of an oscillator [7] in an interesting temperature range of -40 °C to 80 °C. The frequency varies about 43 MHz and the output power about 0.6 dB. This figure shows, that even circuits containing 8 FET devices [7] can be simulated using the proposed scaling functions without any problems. The simulation has been performed using the TOPAS model [3] and HP-EEsofs series IV (libra).

SUMMARY

We presented a FET model, that uses very accurate scaling routines. Furthermore, the same scaling routines are suitable for temperature calculations. Simulations using scaled models show perfect agreement with small signal S-parameter measurement for different temperatures and with noise measurements. The scaling functions have been added to our TOPAS [3] model within HP-EEsofs circuit simulation software series IV (libra).

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FIGURES

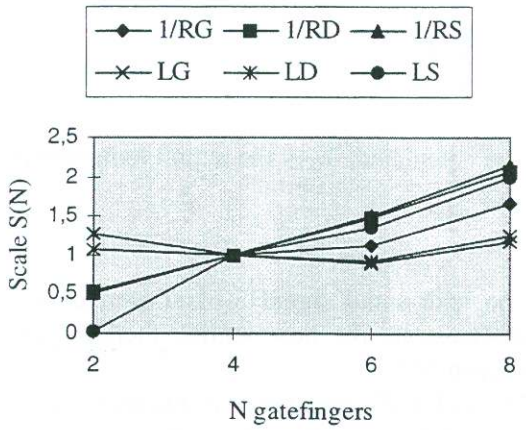

Figure 1: Scaling of extrinsic elements with number N of gatefingers, gatefinger width W_t=40µm.

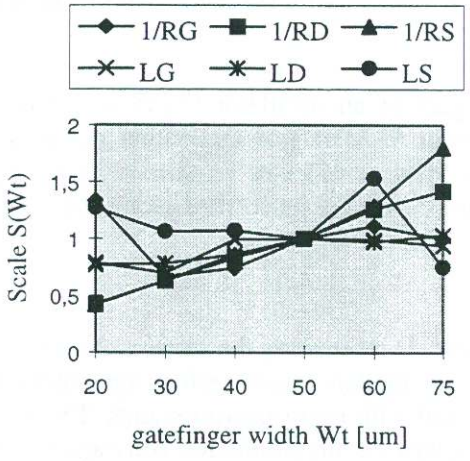

Figure 2: Scaling of extrinsic elements with gatefinger width Wt, number N of gatefingers N=4.

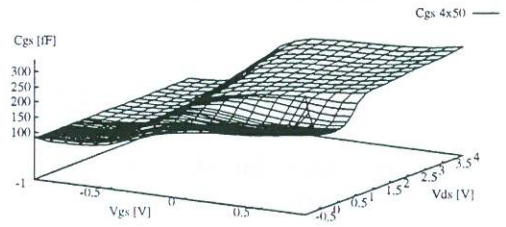

Figure 3: Intrinsic gate-source capacitance for the 4x50 µm HEMT.

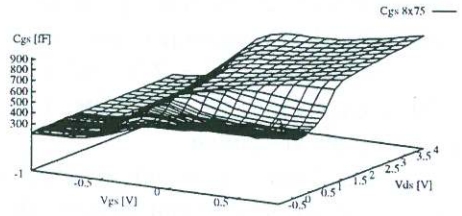

Figure 4: Intrinsic gate-source capacitance for the 8x75 µm HEMT.

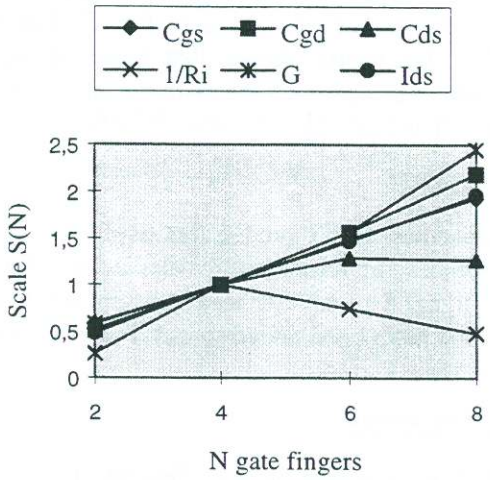

Figure 5: Scaling of intrinsic elements with number of gate fingers N.

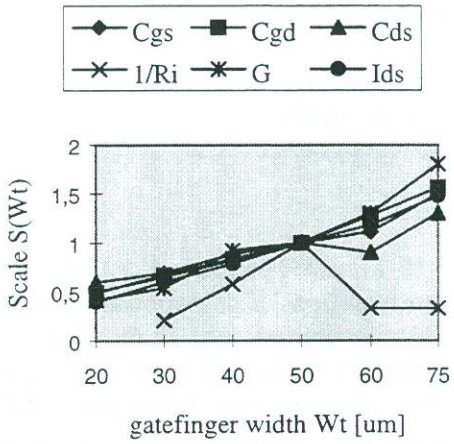

Figure 6: Scaling of intrinsic elements with gatefingerwidth Wt.

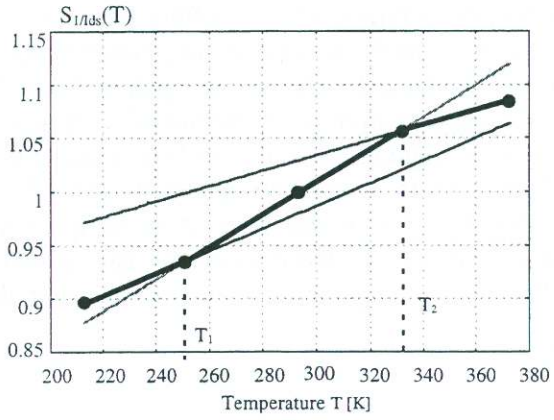

Figure 7: Scaling coefficients and straight lines.

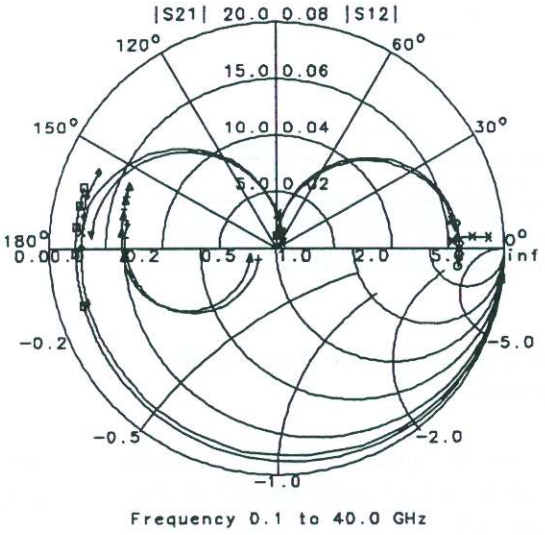

Figure 8: A 4x50µm HEMT scaled to a 8x75µm HEMT at Vgs=0V and Vds=2V.

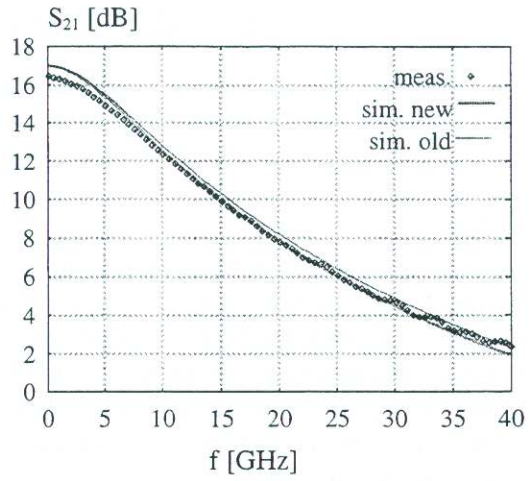

Figure 9: Simulation (simple and new scaling) vs. measurement of S21 of a 4x40µm, HEMT at T=373K. Model has been scaled from a 4x50µm HEMT at T=293 K. Bias point: 0V / 2V.

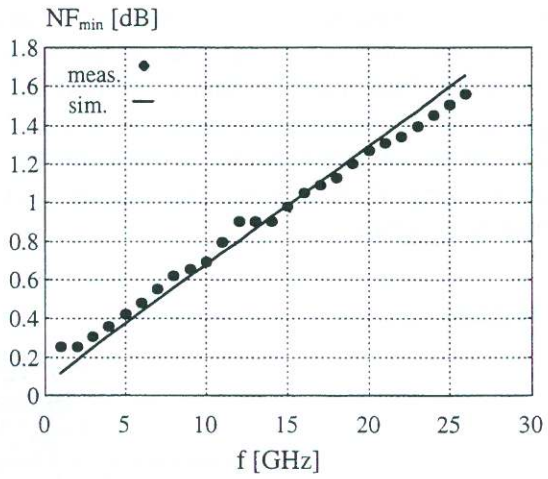

Figure 10: Simulation vs. measurement of NF_{min} of a 4x40µm HEMT at -0.1V / 2 V. Model has been scaled from a 4x50µm device.

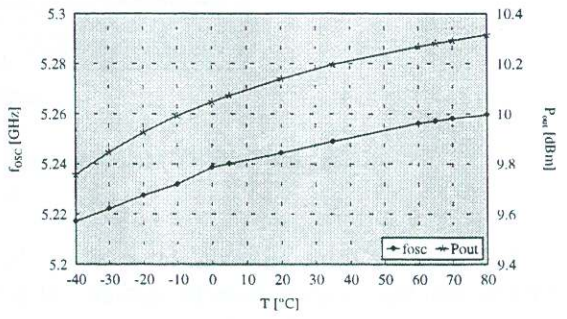

Figure 11: Simulation of oscillator frequency and output power vs. temperature.