NOVEL WIDE BANDWIDTH GAAS SAMPLING MMIC USING MICROSTRIP BASED NONLINEAR TRANSMISSION LINE (NLTL) AND NLTL SHOCK WAVE GENERATOR DESIGN

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ABSTRACT

This paper reports a novel MMIC sampler based on NLTL technology which has been designed using the Philips ED02AH process. The sampling MMIC can be used to measure waveforms in the (3→34) GHz bandwidth. A tapered microstrip based NLTL pulse generator has been combined with a diode-resistor bridge to minimize on GaAs real estate compared to CPW methodology. The advantage of the designed sampling MMIC is wide bandwidth, compressed size and consequently lower cost. The sampling MMIC finds application in sampling oscilloscopes and Time Domain Reflectometers (TDRs). A CPW based NLTL shock wave generator has also been designed for comparison based on bonding several MMIC NLTL samples together.

INTRODUCTION

Compact down converter samplers have found applications in frequency counters, phased locked synthesizers, TDRs and oscilloscopes Whiteley et al (1). The sampling circuit consists of a pulse generator and a diode resistor-bridge. The bandwidth of the sampling circuit is determined by the pulse width and the sampling diode parasitics. The bandwidth (BW) can be approximated as Grove (2) BW (GHz) = 350 / t_g (ps) where t_g is the pulse width. The sampling circuit bandwidth is limited by (35→45) ps fall time generated by the Step Recovery Diode (SRD) (1). NLTL technology increases the sampling circuit bandwidth up to 150 GHz Ruai et al (3). Coplanar waveguide (CPW) based NLTLs have the advantage of planar signal and ground conductors which eases grounding. However CPW based NLTLs occupy large real estate and require large aspect ratios which are difficult and expensive to implement using standard foundries. For example a 40 GHz cut-off frequency, 12 section NLTL is nearly 10 mm long and 0.5 mm wide which is difficult for fabrication. A NLTL based sampler with compressed size and flexible aspect ratio is developed based on microstrip NLTL technology Salameh and Linton (4). This development leads to repeatable design and reduced cost utilizing standard foundries.

The Philips ED02AH BE varactor which has strong nonlinear CV characteristics and 14 V breakdown is integrated within the NLTL structure to produce the required pulse while the 2 x 15 μm ED02AH GM diode which has small junction capacitance is used as a gate (5). The NLTL number of sections was set at 8 to produce a pulse with 17 ps width and 3V height over the (3→6) GHz LO frequency range Salameh and Linton (6). The designed sampling MMIC has a wide band width (3→34) GHz and compressed size due to the use of BE varactors, meander microstrip lines and via holes. The designed sampling circuit can be integrated within TDRs Rodwell et al (7), Ruai et al (8) for small signal characterization of passive and active elements.

In this paper also an 8 section homogeneous NLTL is designed utilising the Philips ED02AH process. This design has the advantage of reducing the required size and not exceeding the maximum allowable aspect ratio for the foundry process. This NLTL finds applications in sampling circuits and Time Domain Reflectometers (TDRs) (8).

SAMPLING MMIC DESIGN

The GaAs sampling MMIC is designed using the Philips ED02AH process. The MMIC layout and circuit diagram are shown in figure 1 (a) and (b). The NLTL is designed using BE-varactors within the ED02AH process which has strong nonlinear CV characteristics, -14 V breakdown and a model valid up to 40 GHz. A 100 Ω characteristic impedance meander microstrip line which corresponds to an 8 μm strip width is designed to provide a time delay between the varactors. The number of sections is set at 8 and the Bragg cut-off frequency is set at 20 GHz to permit pulse generation with 17 ps width and 3 V height over the (3→6) GHz LO frequency range. The

section length and diode area are tapered exponentially to reduce the number of sections required to implement a fixed NLTL length and consequently less via holes are needed for diode grounding with two diodes sharing one via hole. Section lengths and diode areas are computed based on 50 Ω large signal input impedance in order to reduce reflection loss.

The sampling circuit design procedure reported earlier requires a balun differentiator to convert the step signal into two symmetric pulses applied across the sampling bridge (7). The design procedure used in this paper eliminates the need for the balun differentiator by generating a pulse signal directly using a microstrip based tapered NLTL. Also biasing the circuit is simple where a single DC bias at the LO input side of the NLTL is required. Two 2x15 μm GM diodes D_1 and D_2 are used as a gate in the sampling bridge such that the pulse signal is isolated from the RF signal during the off period (when the diodes are off). The resistors R_3 and R_4 are used as loads for the pulse and RF signals respectively. During the on period (when the pulse turns the diodes on) the RF signal partially charges the sampling capacitor C_1 through a 50 Ω resistor. It is necessary that during the off period the capacitor C_1 discharges through a large resistor ($R_1 + R_2$), otherwise C_1 will charge asymptotically to the RF peak. The RF signal should be offset by Δf from nf_o (f_o is the LO frequency and integer n) such that the RF signal is mapped onto an IF frequency with Δf GHz. Charging and discharging of C_1 are shown in figure 2. The capacitor C_2 and the resistor R_2 are inserted to eliminate the high frequency components superimposed on the IF signal. The response of the C_2R_2 low pass filter is shown in figure 3 where the phase is almost linear and the amplitude varies from -0.0007 dB to -0.07 dB over the (1→10) MHz range. This allows an RF signal containing more than 10 harmonics to be mapped to a 1 MHz IF frequency with negligible distortion. The filter distortion effect can be reduced further by reducing the IF frequency. A 40 pF DC block (C_3) is inserted to maintain constant bias across the BE-varactors and to block the bias from the GM-diodes.

SHOCK WAVE GENERATOR DESIGN

The sampler circuit occupied 3x1.4 mm^2 MMIC area. The remaining 3x0.6 mm^2 MMIC area was utilized to design a shock wave generator using the BE-varactors and CPW line as shown in figure 1 (a) and (c). The design procedure is summarized by choosing the cut-off frequency and computing the varactor area, section length and CPW dimensions. The large signal input impedance is set at 50 Ω to improve matching. The CPW characteristic impedance is recommended to be greater than 75 Ω such that the CPW parasitic capacitance to ground is much less than the varactor nonlinear capacitance. The CPW characteristic impedance is set at 100 Ω such that an integer number of sections (8 sections) could be implemented within an available 3mm long MMIC area. This is because more than one sample can then be cascaded and wire bonded to form a longer NLTL. The CPW signal line width is set at 5 μm and the signal ground separation is set at 50 μm to give a 100 Ω CPW characteristic impedance and reduced parasitics between the varactor ohmic contact and CPW ground plane. Since no CPW model is available within the Philips ED02AH process, empirical formulas from the literature are used to construct a CPW model valid up to 100 GHz. The BE-varactor is used as the nonlinear element which has strong nonlinear capacitance, -14 V breakdown and a model valid up to 40 GHz. Consequently the NLTL cut-off frequency is set at 40 GHz. A single finger BE-varactor is implemented parallel to the CPW signal line. This configuration makes the unwanted varactor parasitic inductance usable as part of the required CPW series inductance. Using the previous design parameters, the section length equals 321 μm and the gate length equals 33 μm. The layout of the designed NLTL is shown in figure 1 (a) and (c).

SIMULATION RESULTS

The equivalent model of the MMIC layout is constructed within HP-MDS using the Philips ED02AH models valid up to 40 GHz. The sampling MMIC is excited by a 25 dBm sinusoid superimposed on -1V DC bias. The simulated pulses generated by the NLTL for 3, 4 and 6 GHz LO frequency are shown in figure 4. Using a 4.1 GHz 1 V_{pp} RF signal and a 4 GHz LO frequency, the RF signal is mapped onto an IF signal with $\Delta f = 4.1 - 4 = 0.1$ GHz at the output as shown in figure 5. The RF signal and its corresponding IF signal are nearly the same with attenuation due to the diode sampling bridge and the R_2C_2 low pass filter. The 3 dB bandwidth of the sampler is defined as the frequency at which the output IF voltage drops 3 dB below the low frequency value (2). Simulation results showed 34 GHz 3 dB bandwidth. The RF signal when composed of more than one harmonic suffers from shape distortion due to the frequency response of the sampler as shown in figure 6. A calibration procedure can be performed to compensate for the frequency response by computing the attenuation and the phase between the RF and IF signals over the (3→34) GHz bandwidth.

The CPW model is constructed within HP-MDS using empirical formulas from the literature valid up to 100 GHz Frankel et al (9), Gopinath (10). The Philips model for the BE-varactor available within the Philips ED02AH-MDS library is used to construct a NLTL model. The bond wire between adjacent samples is modeled based on measurements. The HP-MDS transient simulator known as HP-Impulse is used to simulate the nonlinear structure versus number of samples.

Ten hours are needed to simulate a six stage assembly (48 sections) NLTL excited by a 27 dBm sinusoidal signal superimposed on a -3 V dc bias over (0→1100) ps time interval with 2 ps time step. This length of time is needed because the exact Philips varactor model is used in simulation. To reduce the simulation time, the exact varactor nonlinear CV characteristics are approximated using a hyperbolic fit. A hyperbolic fit is used since it has fast convergence which is constructed as a substitute to the exact model and just 10 minutes are needed to simulate the same structure. The reduction in simulation time is at the expense of accuracy as shown in figure 7 where 7 ps fall time is obtained. The difference between the simulated output waveforms using the exact and the approximate models is small as shown in figure 7 compared with the large reduction in simulation time (from 10 hours to 10 minutes).

MEASUREMENTS

Large signal measurements have been performed for an 8 section, 30 GHz Bragg cut-off frequency, microstrip based NLTL pulse generator using the MTA. Two port forward calibration was performed using Sort-Open-Load (SOL) standards over the (2-40 GHz) frequency range. The large signal measurement apparatus is shown in figure 8. The output harmonics are measured for different input frequencies at 20 dBm input power and the output waveform is extracted using Fourier series. The measured and simulated output pulses are shown in figure 9 where 1.8 V pulse height and 19 ps pulse width are obtained for an 8 GHz input frequency and 1.2 V pulse height and 18 ps pulse width are obtained for 10 GHz input frequency. The pulse generator is able to produce pulses with an amplitude of 3 V and a pulse width of 6 ps for a 23 dBm input signal. The maximum output power of the HP amplifier is 23 dBm and due to losses only 20 dBm is obtained at the probe tips.

CONCLUSION

A low cost compressed size sampling MMIC has been designed using the Philips ED02AH process. Microstrip line technology can be used as an alternative to the CPW for NLTL design with the advantage of reduced size and flexible aspect ratio. The microstrip based sampling MMIC can be utilized in a TDR using two diode/resistor bridges and an attenuator which can be used for small signal characterization of passive and active elements over the (3→34) GHz frequency range. The RF amplitude should be less than 0.5 V across the sampling bridge to ensure that the RF signal does not bring the sampling diodes into forward conduction.

A long NLTL structure which is able to generate a shock wave with 7 ps fall time out of a 27 dBm, 2 GHz sinusoidal signal can be implemented by bonding several short NLTL MMIC stages. This technique has the advantage of reducing the required MMIC area and avoiding strict foundry aspect ratios. Exact varactor CV characteristics require very long simulation time while using an approximate hyperbolic fit reduces the simulation time significantly and permits simulation of longer NLTL structures.

ACKNOWLEDGMENT

This work is supported by ASAI, AB and ORS. The authors thank Derek Smith at PML for his assistance.

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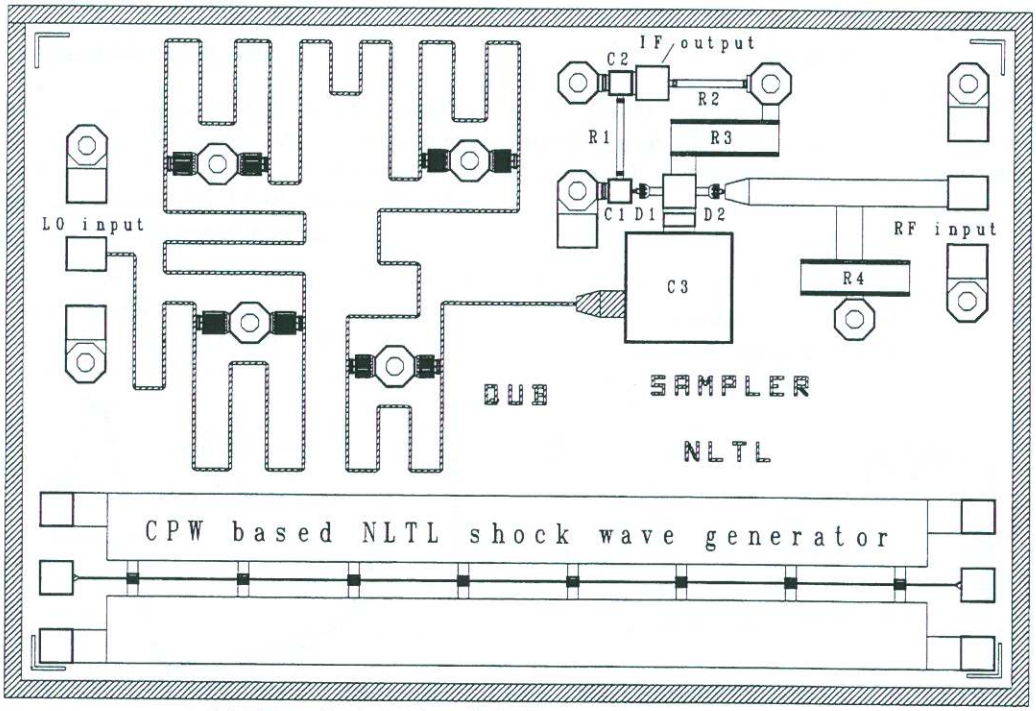
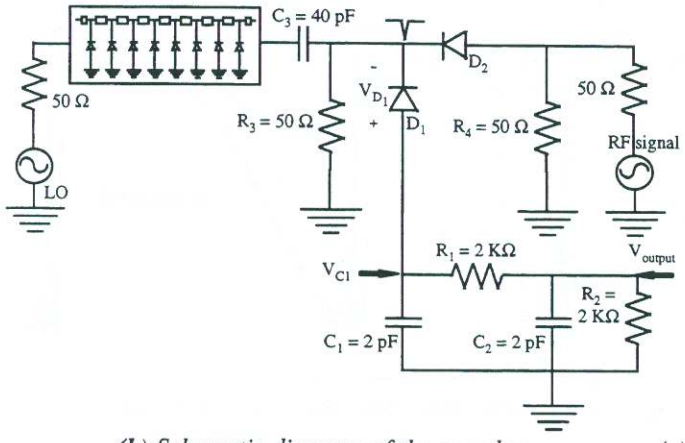
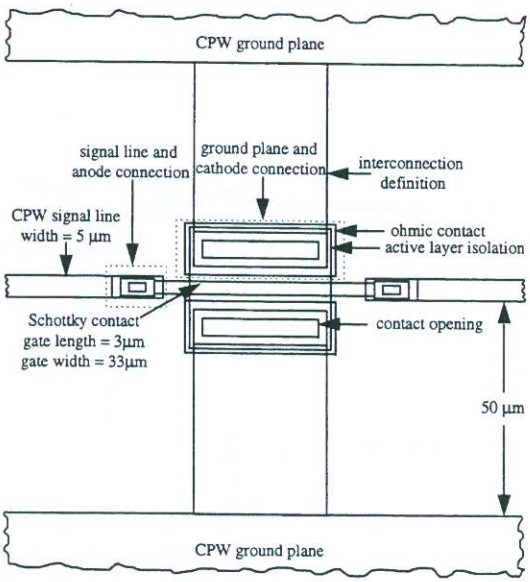


(a)) Sampler (top) and shock wave generator (bottom)



(b) Schematic diagram of the sampler



(c) Magnified view of the shock wave generator

***Figure 1 (a)** Sampler (top) and shock wave generator (bottom) laid out on 3x2 mm MMIC area*
***(b)** Schematic diagram of the sampler **(c)** Magnified view of the shock wave generator.*

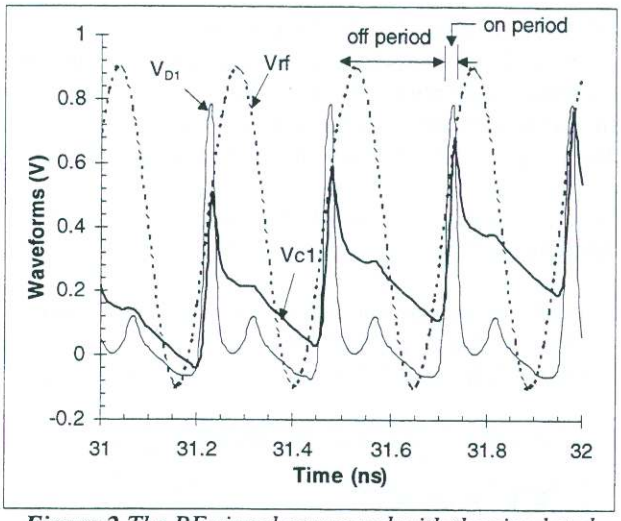


Figure 2 The RF signal compared with the simulated waveform across C_1 showing charging of C_1 during the on period and discharging during the off period. The pulse signal is also shown.

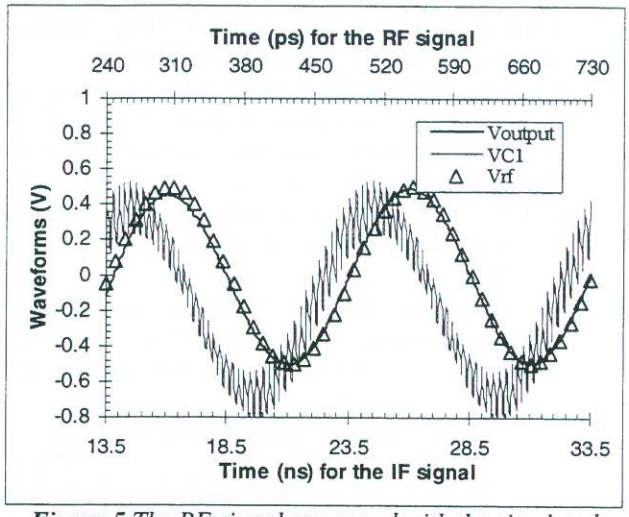


Figure 5 The RF signal compared with the simulated output waveform, the wave form across C_1 (lower scale) is also shown. The output waveform is scaled by 16.3 to ease comparison with the RF signal which can be considered as a calibration parameter.

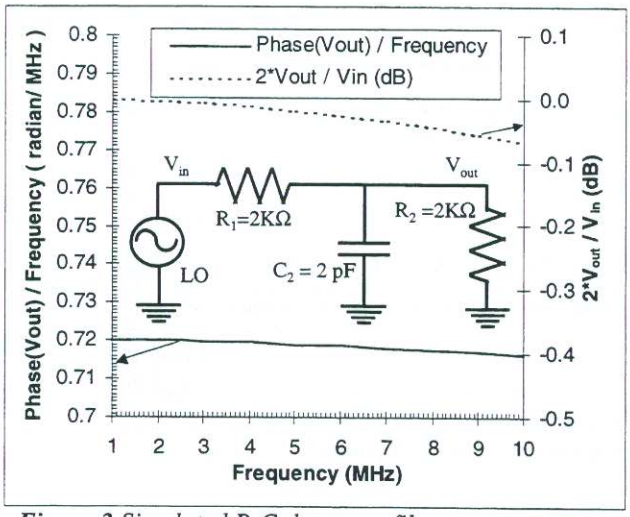


Figure 3 Simulated R_2C_2 low pass filter response versus IF Frequency.

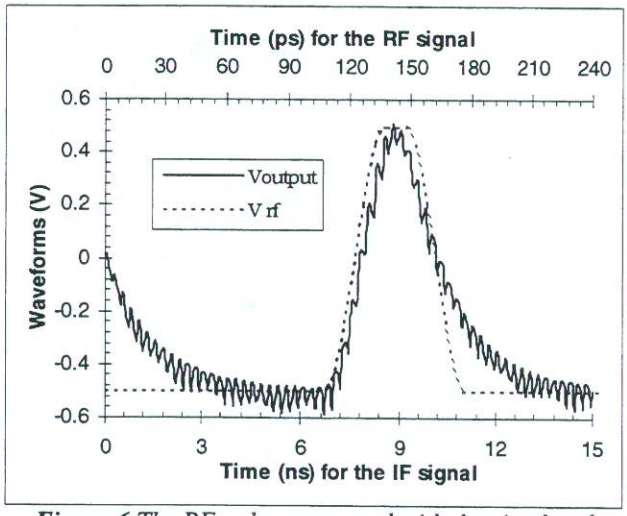


Figure 6 The RF pulse compared with the simulated output waveform. The output waveform is scaled by 23 to ease comparison with the RF pulse

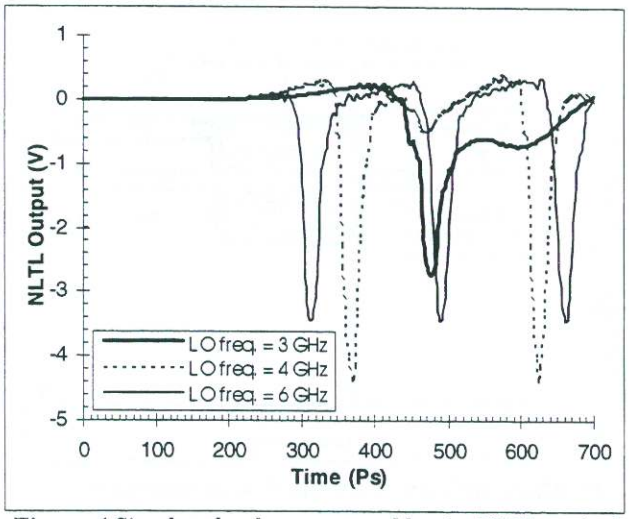


Figure 4 Simulated pulse generated by the NLTL excited by 25 dBm sinusoidal signal superimposed on a -1 V dc bias for 3, 4 and 6 GHz LO frequencies.

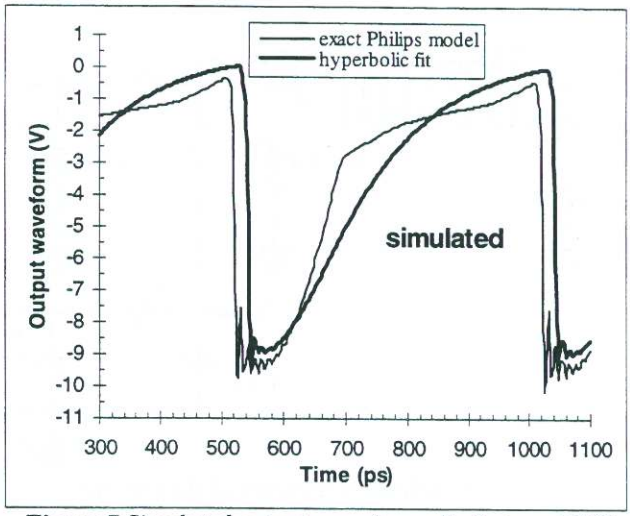


Figure 7 Simulated output waveform of a 6 stage CPW NLTL (48 sections) excited by a 27 dBm, 2GHz sinusoidal signal superimposed on a -3 V dc bias using the exact Philips model and the approximate hyperbolic fit.

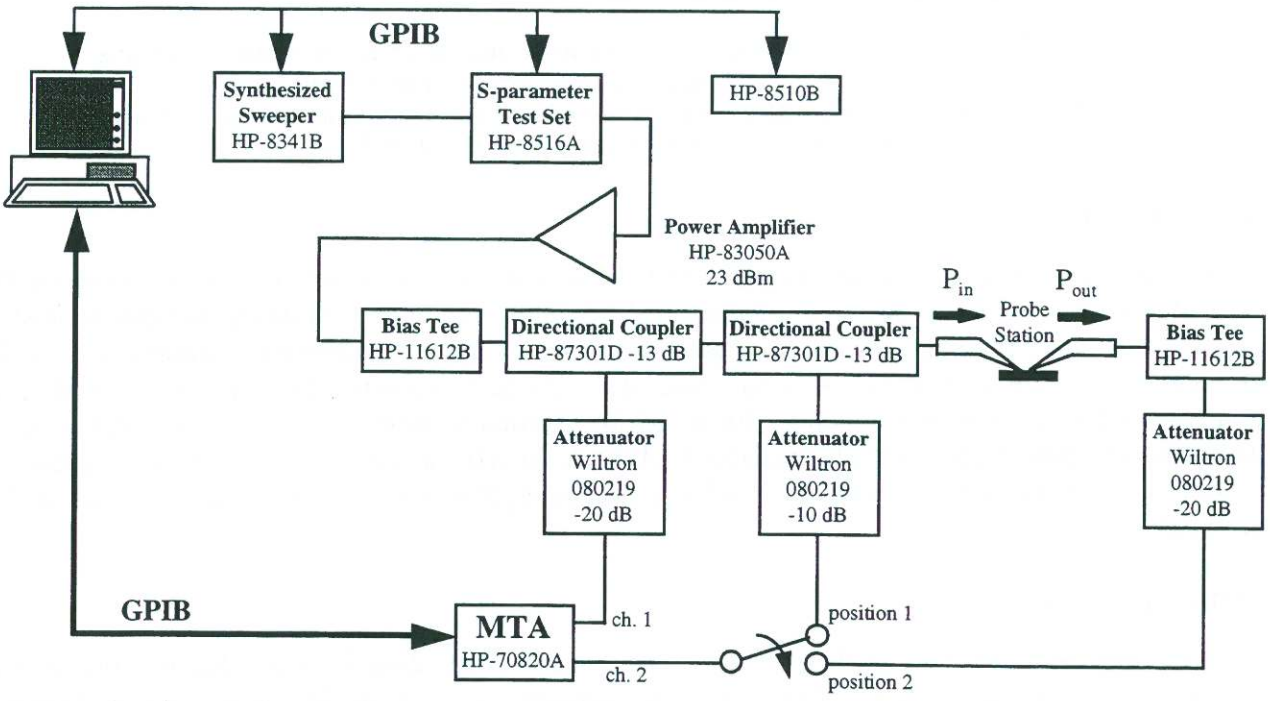
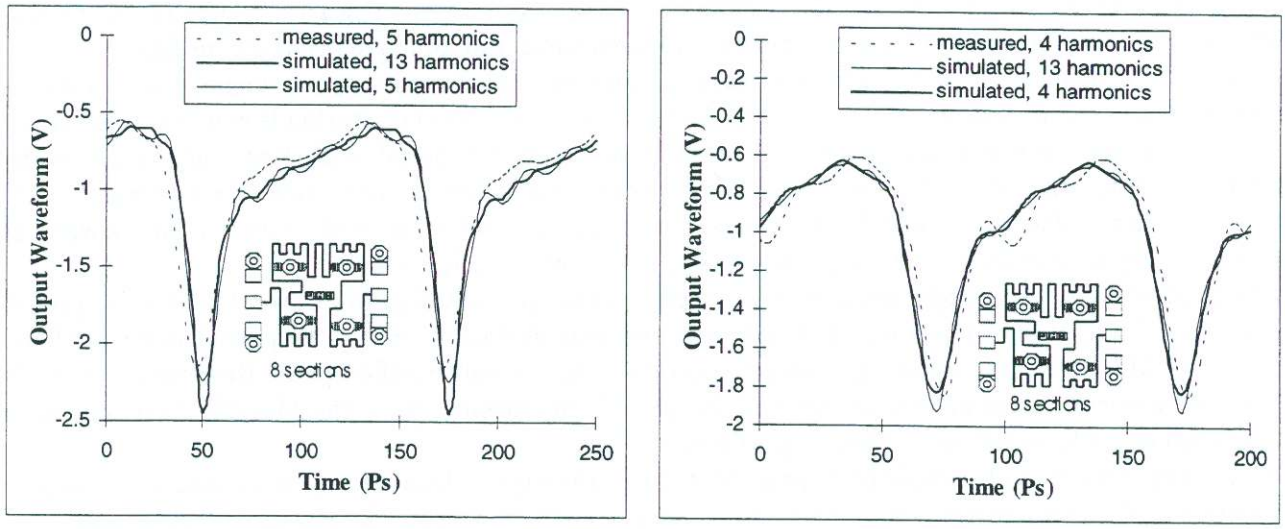


Figure 8 *Large signal measurement set-up.*



(a) *8 GHz input frequency* ***(b)*** *10 GHz input frequency*

Figure 9 *Measured and simulated output waveform of the 8 section microstrip based GaAs MMIC tapered NLTL pulse generator fabricated utilising the Philips ED02AH process for a 20 dBm sinusoidal signal superimposed an a -1 V DC bias* ***(a)*** *8 GHz input frequency* ***(b)*** *10 GHz input frequency.*