A NEW HIGHLY LINEAR MMIC SINGLE SIDE-BAND CONVERTER FOR DIGITAL RADIO LINKS

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ABSTRACT

This paper describes the design of a very compact Monolithic Single Side-band (SSB) Mixer for Digital Radio Links. The mixer can be used in transmitters as an SSB up-converter over the 5.6÷8.5 GHz range, but also in receivers as down-converter combined with Low Noise Preamplifier. All the sub-circuits except only the IF hybrids, are included in a unique small chip whose total size is 3.556 x 3.556 mm^2. Very high Linear operation with more than 29dB of Image Rejection and 27dB of Carrier suppression, is achieved over the whole operating band.

INTRODUCTION

Fiber optic has increasingly become the preferred medium for high capacity transmission systems, but the benefit of microwave radio link such as security, speed of deployment and economics, are still strongly appreciated by networks planners. To permit a successful integration into modern synchronous networks, more sophisticated radio equipment designs are requested with higher performances and miniaturization, but lower manufacturing cost.

A new family of cost-effective digital radio relay equipments, characterized by a very high level of integration, is now under development with the following main requirements :Design unification and component standardization, Size reduction, Manufacturing modularity and Testing time reduction.

In [1] the efforts for assembling some techniques and methodologies addressed to fulfil these requirements were presented, with the development of a new MMIC-based Power amplifier structure for transmitters. The next step undertaken is the integration of the up-converter to the Power amplifier structure. To do this, a new MMIC has been designed and is presented for the first time in this paper. High linearity, wide band of operation, possibility to use the same MMIC both as up-converter and down-converter and small size, are the main objective for this design. After a description of the basic configuration and operating principle of the mixer, a detailed examination of the MMIC design is reported. The layout is described and circuit simulation are presented. Finally, some conclusions are reported.

CONFIGURATION AND OPERATION PRINCIPLES

The block diagram of the basic SSB circuit is shown in figure 1. It consists of two identical mixers, an in-phase RF Power combiner/divider and two quadrature hybrid, one for the LO, the other for IF signals. To isolate the LO from the RF, a Double Side-band Balanced-type (DSB) mixer is employed. The unbiased channel of a MESFET (cold FET) was chosen as the mixing element because of the very low intermodulation value that can be achieved with a small amount of LO Power [2]. The cold FET operates near pinch-off condition as a simple resistor whose resistance is only very weakly non Linear when varied by applying the LO signal to the gate.

Further on, there is an intrinsic isolation between the LO and RF/IF signals applied to the drain of the FET.

In the DSB mixer the LO signal, split by a 180° hybrid, is driven into the gate of the two cold FET, the IF and RF are connected to the drain terminals. The two RF are matched by an in-phase Power combiner/dividers and the two IF by a 180° hybrid.

For up-conversion operation, an IF modulating signal is fed to the mixers through the quadrature IF hybrid (I and Q), generating out the up-converted Upper Side Band (USB) and Lower Side Band (LSB). Applying these signals to an RF in-phase combiner results in a single side-band suppressed carrier output, without the use of any filters.

Either the lower or upper side-band, can be generated by inverting the I and Q signals.

For down-converting operation a small RF signal is fed to the mixers through the in-phase Power divider resulting out in two IF output signals of equal magnitude but in phase-quadrature. Applying these signals to an IF quadrature hybrid, the signals coming from the two RF side bands appear separated at the two outputs of the hybrid.
The LO cancellation is realized by the DSB mixer section mirroring two single resistive equal mixers driven at the gate by two equal LO signals in phase opposition and at the drain with two equal IF signals in phase opposition and the image rejection by mirroring the two DSB mixer with two quadrature LO and IF signals.
Actual circuits realize the mirror configuration scheme only with a certain degree, so an amount of the undesired side-band and carrier will appear at the output of the converter depending on the overall amplitude and phase unbalances. For this aspect the use of monolithic technology is a good choice providing a much better match between the two halves of the circuit in comparison with MIC technology.

MMIC DESIGN

Two balanced mixers are utilized in the SSB converter. They employ cold MESFET in common source configuration as Voltage Controlled Resistor, for mixing the different signals, with the LO applied to the gate and the RF/IF path connected to the drain. High-pass and low-Pass basic filters are used to easy isolate the IF port from the RF port.
All the necessary sub-circuits such as RF in-phase Power combiner/divider, LO quadrature hybrid, 180° hybrid, biasing circuits and balanced mixers, are included inside the chip. Only the needed IF hybrids are external components. To allow the use of the mixer as both up and down converter, all the sub-circuits are realized with passive networks.
In MMIC technology, at frequency below 18 GHz, distributed elements consume too much valuable GaAs surface area to be cost-effective. An appreciable reduction in area without a degradation in electrical performances can be realized with the use of lumped elements [3]. All the passive networks implemented in this MMIC are designed using lumped elements with the specific aim of being particular process-tolerant and allowing one-octave bandwidth operation.
A 180° hybrid is used as part of the balanced mixer and a quadrature hybrid is required to split the LO signal in two components of the same amplitude but phase shifted of 90°.
The conventional "rat-race" structure, consumes too much area at these frequencies, so a broad-band lumped-elements realization of the "rat-race" [3] is used with very good results either for the LO 180° or for 90° hybrid. A three-way lumped-element Wilkinson coupler was adopted, followed by two all-pass networks designed in order to shift each other respectively +90°/-90° and +45°/-45°, keeping an appropriate impedance matching, as shown in figure 2 and figure 3.
The in-phase Power combiners/dividers needed for extracting/applying the RF signal were also realized by a lumped-element network. The one for the DSB section is realized as just two capacitor matched together with microstrip lines at one end. The capacitor acts as an high-pass filter : a RF (high frequency) short-circuit and IF (low frequency) open-circuit . The two IF ports will act as an IF short-circuit and an RF open-circuit when externally properly filtered by a low-pass IF L-C section. This section acts as an in-phase combiner/divider for the RF signal generated/injected while keeping isolated the two IF ports with respect to the RF port and providing as output matching the two cold FET. The scheme is shown in figure 4. The one for the SSB section is instead realized as a Wilkinson type network providing a 50 Ω output matching, as shown in figure 5. The electrical ideal lumped elements scheme is shown in figure 6.

CIRCUIT SIMULATION

Using a commercially harmonic balance non-Linear simulator the matching networks were designed and the overall mixer performances simulated. We used the unbiased channel of a 300μm 0.5μm MESFET as a simple resistor mixing element whose resistance can be varied by the gate voltage swing signal. The models of active device and passive elements used (inductors, capacitors, resistors and via holes) are taken from a Foundry Manual Library [5]. We started first with the optimization as an ideal lumped circuit, composed just from active device and ideal L-C-R components. Then we made the optimization with the Foundry active/passive electrical models. Finally we made an optimization taking into account for all the parasitic microstrip components introduced by the layout constraints. Using an electromagnetic simulator we took into account the effects of electromagnetic coupling between the various circuits elements on MMIC design. Extensive simulation were made in order to reach the maximum performances of the final mixer versus layout parasitic, possible coupling effects and process

related variation. Wide-band performances were obtained from the hybrid networks together with control on maximum off-amplitude and phase unbalance.
The lumped-element 90° hybrid for the LO in the SSB configuration and the lumped-element 180° hybrid for the LO in the DSB mixer, so designed, configuration keep the phase/amplitude unbalance into a ±4°/± 0.1 and into ±3°/ ± 0.1 respectively, over the 5.6-8.5 GHz band, as shown in figure 7 and 8.
The DSB mixer was optimized in order to achieve the LO carrier suppression while keeping the lower (LSB) and upper (USB) side-band equally balanced. Then the image rejection was obtained mirroring the two DSB mixer as shown previously. The SSB mixer was then optimized with the 90° LO hybrid and the in-phase combiner/divider at the output. The LO and RF return loss was kept low enough for either up-conversion or down-conversion operation.
We simulated the whole mixer configuration with the IF hybrids and filters included. In figure 9 the simulated up-conversion USB mode operation is reported, with an LO level of +16dBm , an IF of -5dBm at 140MHz and V_{gs}=-1.65V, in the 5.6-8.5 GHz band. A conversion loss close to 10dB with a LO carrier suppression better than 27dB and an image rejection (LSB rejection) more than 29dB are obtained. Figure 10 shows the IF/RF and LO/RF isolations better than 49dB and 57dB respectively, for a very large band, for the up-conversion USB mode operation. Figure 11 shows the Pin/Pout characteristic for the USB Up-Converter mode operation with an LO=+16dBm and V_{gs}=-1.65V. The picture show the Power USB, Conversion Loss, the LO carrier Suppression and Image Rejection behaviour by Power sweeping the IF, showing a P_{1dB} better than -2.5dB over the band as shown in Table 1. As can be seen from figure 11, the LO carrier suppression remains at values less than 20dB and the image rejection better than 35dB, with USB RF output Power till to -20dBm, corresponding to an IF Power level of -10dBm. As the P_{1dB} is better than -2.5dBm, as the IF Power level of -5dBm correspond to an RF output Power close to -15dBm that is better than 12.5dB back-off , so allowing very high Linear operation [2,4].
The same characteristics can be achieved for the LSB Up-Converter mode by inverting the 90° IF hybrid.
The down-conversion mode operation is obtained by injecting an RF signal and extracting the low frequency IF LSB or USB band. Figure 12 show the conversion loss of the down-converter with LO=+10dBm, RF=-10dBm and Vgs=-1.65V in the 5.6-8.5 Ghz band. The LO is set to provide an IF equal to 140MHz. The conversion loss so obtained is close to 10dB. A Low noise Preamplifier will drive the down-converter mixer with higher level than that at the antenna values. Figure 13 shows the Pin/Pout characteristic of the down-converter mode operation, showing a conversion loss better than 11dB and an IF output power at 1dB compression point better than -9dBm, with an LO=+10dBm and Vgs=-1.65V.

LAYOUT

The layout was carried out paying particular attention to the symmetry of the two mixer section so that the amplitude and phase balances would be maximally preserved. We positioned the various elements in order to avoid e.m. parasitic coupling. In order to fulfil the low cost requirement, a very compact layout was designed with total size 3.556x3.556mm^2. Great attention was posed on LO,RF and IFs pads positioning , via holes distances, bias circuit drawing and circuit symmetry. The main effort was to keep appropriately distances between the various section of the circuit, in order to avoid mutual coupling. The circuit is planned to be fabricated using a 0.5μm D-Mode MESFET process particularly suited for low mixer conversion loss and contains 4 MESFETs, 32 spiral inductors, 31 MIM capacitors, 8 NiCr resistors and 26 via holes for grounding . The final layout outline draw is reported in figure 14.

CONCLUSION

A very compact MMIC Single Side-band Mixer with interesting behaviours has been designed. The mixer new configuration permits either up-converter or down-converter mode operations well suitable for digital radio links use, with a very large band operation. The simulation takes into account the active and passive real MMIC technology components in industrial use. The simulations are aimed to develop the real mixer component so taking care for e.m. MMIC typical encountered constraints and process related variations. The present design is under development for internal microwave module use for a new generation of digital radio links next proposed on the market.

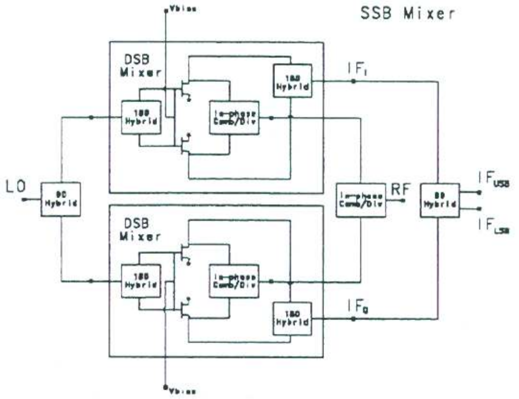

Fig. 1 - SSB Mixer Configuration

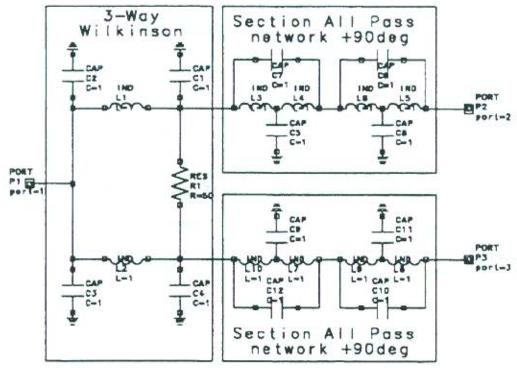

Fig. 2 - LO lumped-elements 180° Hybrid

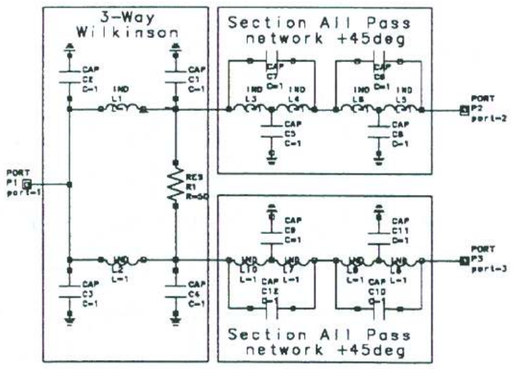

Fig. 3 - LO lumped-elements 90° Hybrid

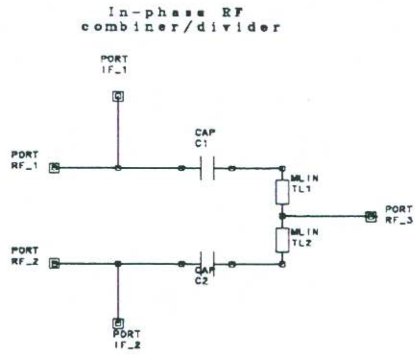

Fig. 4 - In-phase combiner/divider for DSB mixer

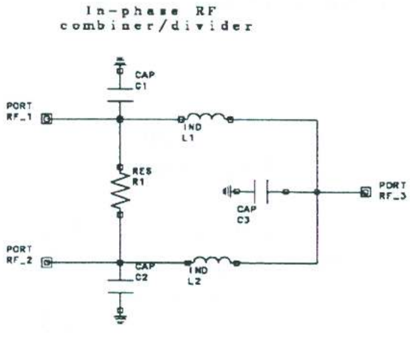

Fig. 5 - In-phase combiner/divider for the SSB section

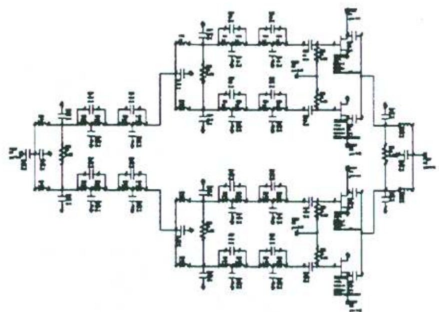

Fig. 6 - Lumped-element MMIC SSB mixer section

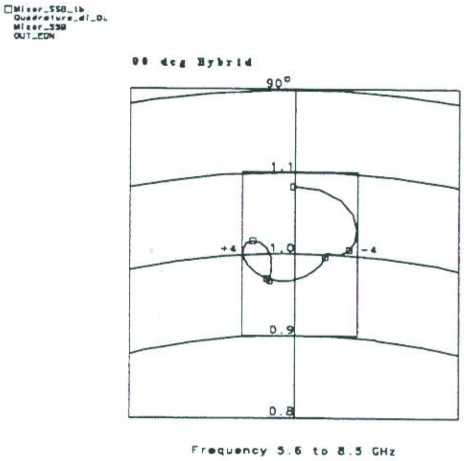

Fig. 7 - Lumped-element 90° hybrid phase / amplitude unbalance

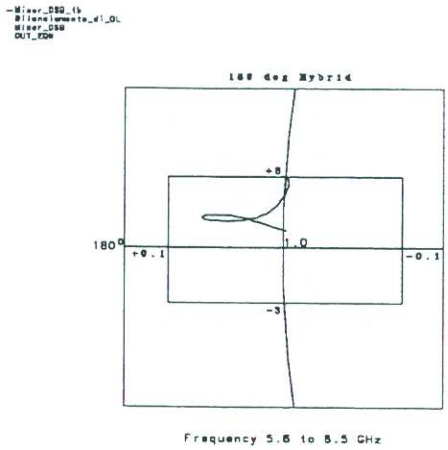

Fig. 8 - Lumped-element 180° hybrid phase / amplitude unbalance

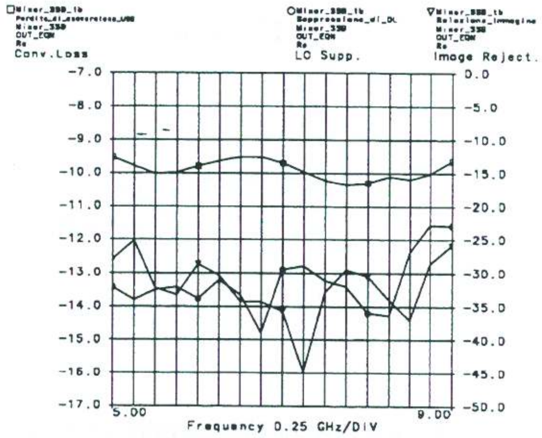

Fig 9 - USB Up-Converter Conversion loss Carrier Suppression and Image rejection. LO=+16dBm,IF=-5dBm,Vgs=-1.65V

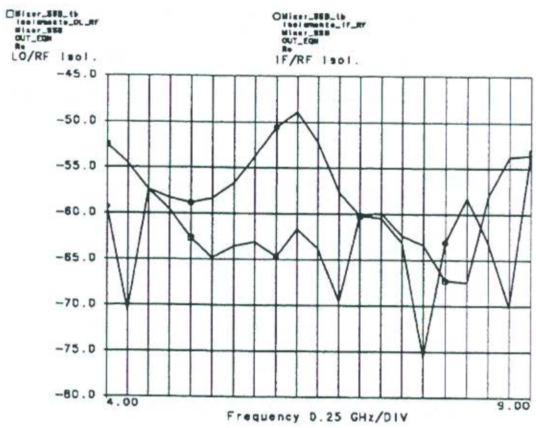

Fig. 10 - USB Up-Converter LO/RF and IF/RF Isolation. LO=+16dBm,IF=-5dBm

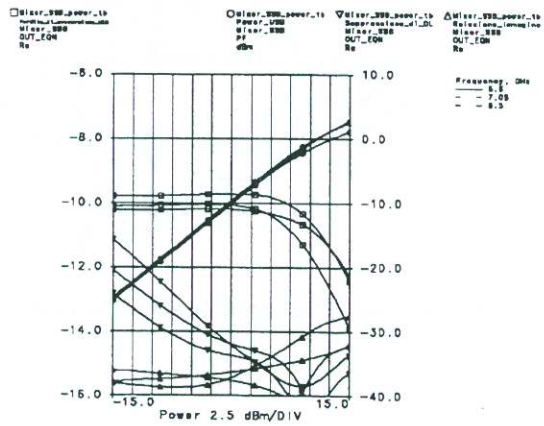

Fig. 11 - USB Up-Converter Pin/Pout characteristics at LO=+16dBm ,Vgs=-1.65V

At LO=+16dBm
Vgs=-1.65V

f [GHz]	Conv.Loss [dB]	P1dB [dBm]
5.6	10.1	-2.5
7.05	9.8	0.0
8.5	10.2	+0.76

Tab. 1 - USB Up-Converter Pin/Pout characteristics

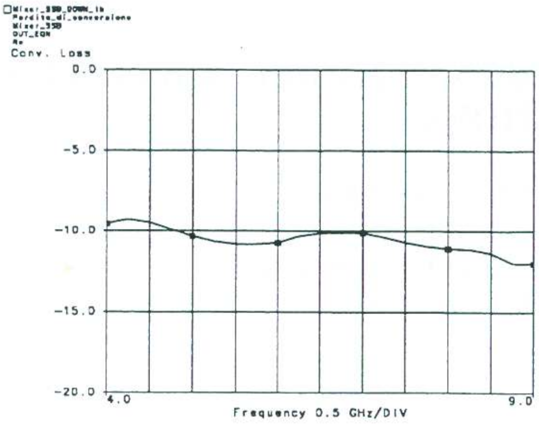

Fig. 12 - Down-Converter Conversion Loss with LO=+10dBm ,RF=-10dBm,Vgs=-1.65V

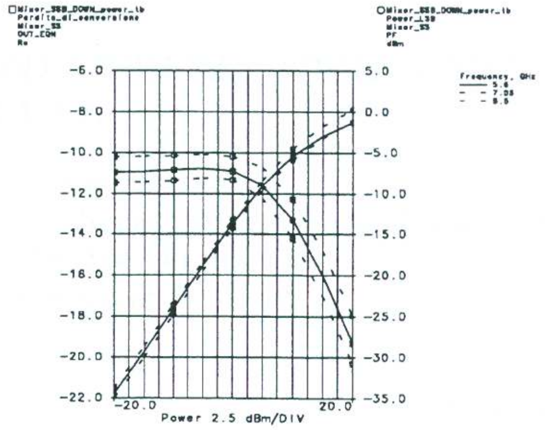

Fig. 13 - Down-Converter Pin/Pout with LO=+10dBm , Vgs=-1.65V

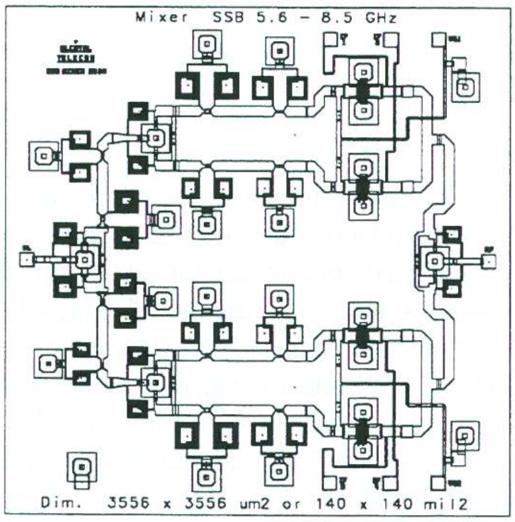

Fig. 14- MMIC SSB mixer layout

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