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DUAL GATE PSEUDOMORPHIC HEMT FOR LOW NOISE AMPLIFICATION IN MILLIMETER WAVE RANGE

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Abstract

The purpose of this paper is to show the capabilities of the dual gate transistors for low noise amplification in the millimeter wave range. Single and dual gate 0.12µm AlGaAs/InGaAs/GaAs pseudomorphic HEMTs have been designed and realized for this study. On wafer S-parameters have been performed up to 110GHz. The current gain cutoff frequency f_T is 70GHz and the maximum available gain is 13dB at 60GHz. A very low minimum noise figure of 1dB is obtained with an associated gain of 20dB at 18GHz. Some others good performances are presented.

Introduction

It is known that the use of high electron mobility materials and the reduction of the dimensions, particularly the gate length of FETs, constitute the two necessary rules to improve the performance of transistors. Pseudomorphic HEMTs with InGaAs channel on GaAs are proven to be suitable up to the millimeter wave range.

The achievement of better results seems actually to be braked, not only by technological difficulties due to the ultra-short dimensions (0.1µm or less), but mostly, by behavioral troubles linked to the short-channel effects [1]. These effects are usually emerged as an increase in output conductance, and so as a shift in the pinchoff voltage with V_{DS} bias. Another consequence is a relatively poor transconductance, because the aspect ratio becomes smaller.

By short-circuiting the second gate of a dual gate transistor, and due to its intrinsic cascode configuration, this device can constitute an interesting solution for solving these problems [2]. Indeed, the analysis of the simplified intrinsic equivalent scheme (Fig. 1) shows that this device composed by two stages (common source and common gate) can be considered, in low frequency range, as equivalent to a single gate FET, whose the main intrinsic elements are written :

$$gd \approx gd_1 \cdot \frac{gd_2}{gm_2 + gd_2 + gd_1}$$

$$Cgd \approx Cgd_1 \cdot \frac{gd_2}{gm_2 + gd_2 + gd_1}$$

$$gm \approx gm_1 \cdot \frac{gm_2 + gd_2}{gm_2 + gd_2 + gd_1}$$

$$Cgs \approx Cgs_1 + Cgd_1 \cdot \frac{gm_2 + gd_1 + gm_1}{gm_2 + gd_2 + gd_1}$$

It appears that smaller output conductance gd and feedback capacitance Cgd are obtained in comparison with an isolated single gate FET. If the value of the transconductance gm slightly decreases, the improvement of gd and Cgd are more important, that leads to produce higher gains. For instance, the intrinsic maximum stable gain MSG, given by

$$MSG = \underbrace{MSG_{FET1}}_{\text{common source}} \cdot \underbrace{MSG_{FET2}}_{\text{common gate}} \approx \left(\frac{gm_1}{\omega \cdot Cgd_1}\right) \cdot \left(1 + \frac{gm_2}{gd_2}\right)$$

is theoretically greater, because of the common gate stage contribution with the $(1+gm_2/gd_2)$ term, which can reach values close to 10.

Unfortunately, we notice that the input capacitance Cgs increases because of the Miller effect, which tends to limit the cutoff frequency of the current gain.

Moreover, this kind of devices presents also the advantage of being very compact and so easily integrable for microwave circuits, and the presence of the second gate allows to design particular applications like among others controlled gain amplifiers.

So, the purpose of this paper is to evaluate comparatively the performance of single and dual gate 0.12µm AlGaAs/InGaAs/GaAs pseudomorphic HEMTs, realized in our laboratory, for applications as low noise amplifiers in the millimeter wave range.

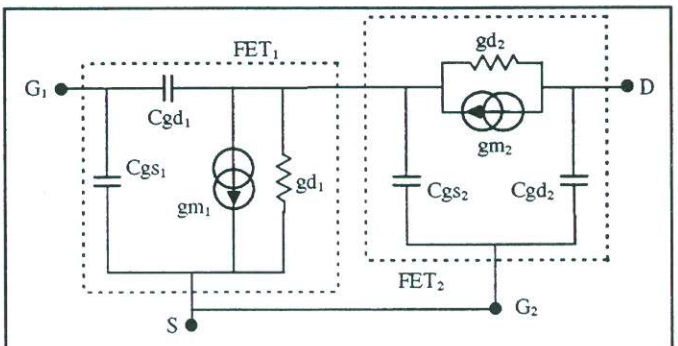

Fig. 1 : Intrinsic equivalent scheme of a dual gate FET in cascode configuration.

Devices design and fabrication

The devices are fabricated on a layer grown by Molecular Beam Epitaxy. A cross section of the layer is shown in Fig. 2. It consists of a 5000Å undoped GaAs buffer grown on a semi-insulating GaAs substrate, a 120Å undoped $In_{0.2}Ga_{0.8}As$ channel, a 20Å undoped $Al_{0.2}Ga_{0.8}As$ spacer, a Si planar doping of 6 $10^{12}cm^{-2}$, a 120Å undoped $Al_{0.2}Ga_{0.8}As$ Schottky barrier and a 500Å n^+- GaAs contact layer. Typical Hall measurements for such a layer demonstrate a 2-DEG concentration of 2.3 10^{12} cm^{-2} with a mobility of $6500cm^2/V.s$ at room temperature.
Conventional 0.12µm gate length technology has been developed for this purpose. HEMTs are fabricated by a mixing of electron beam and optical lithography.
After the deposition of Ni/Ge/Au/Ti/Au and lifted-off, the ohmic contacts are alloyed at 400°C during 40 seconds using a rapid thermal annealing. A 0.09Ω.mm typical value of the contact resistance has been measured.
The MESA isolation and the symmetrical gate recess are realised by $NH_4OH:H_2O_2:H_2O$ wet etching. The 0.12µm long gates were defined by e-beam lithography and a copolymer-PMMA bi-layer photoresist process. The Ti/Pt/Au gates metallisation is supported by silicon nitride and their mushroom shape allows to reduce the gate metal resistance. The distances from $Gate_1$ to the source contact and from $Gate_2$ to the drain contact have been fixed to 0.4µm. Different intergate spacings (0.3µm, 0.5µm and 0.8µm) have been retained.
A 5000Å Ti/Au level was evaporated and lifted-off for metallisation. A 1500Å Si_3N_4 layer was deposited for the active zone passivation and for the dielectric of the 2pF MIM (Metal-Insulator-Metal) capacitors used for the second gate RF grounding.
Finally, a last 5000Å Ti/Au layer is achieved for the MIM capacitors top metallisation, and for the contact pads used for adjusting the second gate bias.
These specific dual gate transistors are available with different gate widths of 2x20µm, 2x30µm and 2x40µm.
On the same wafer are included a 2x40µm single gate FET fabricated for comparison, and a particular dual gate FET whose the second gate is directly connected to the source, so without MIM capacitor. This last one can be interesting for applications which don't need a second gate voltage control, because it becomes as compact as a single gate FET by keeping the cascode configuration properties.
Fig. 3 presents the dual gate devices topologies with and without MIM capacitors.

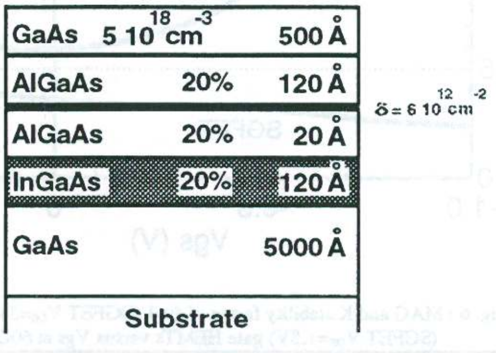

Fig. 2 : Cross section of the layer used for the dual gate transistors realisation.

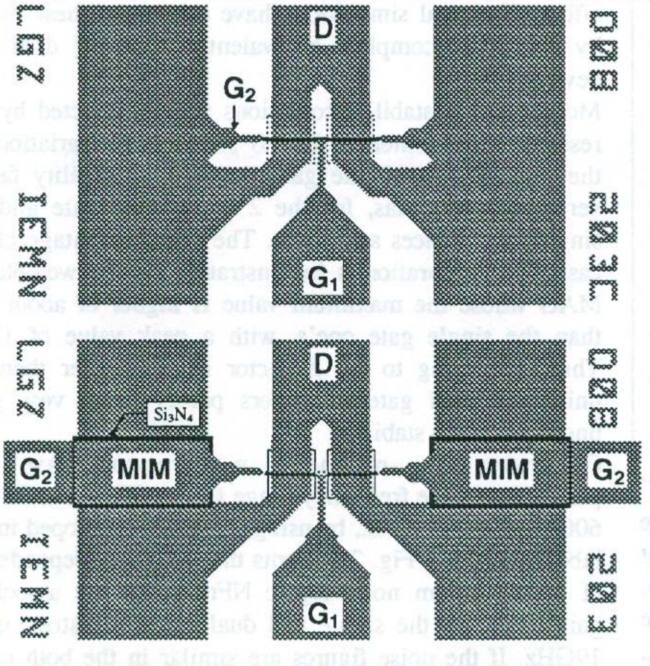

Fig. 3 : Topologies of dual gate transistors with and without MIM capacitors for the second gate RF grounding.

Performance

The S-parameters of the devices have been measured up to 110GHz by using an on-wafer probe station.
The equivalent scheme of transistors are extracted with the well-known Dambrine's procedure [3]. Single and dual gate FETs exhibit respectively maximum extrinsic transconductances of 900mS/mm and 820mS/mm. Fig. 4 presents the typical variations versus V_{GS} bias of the main intrinsic elements (gm, gd, Cgs and Cgd), for the single and the dual gate FETs. These results confirm clearly the theoretical predictions, because a large improvement of the output conductance gd and the feedback capacitance Cgd is obtained for the cascode configuration. A small degradation of the intrinsic transconductance gm is logically observed (1070mS/mm instead of 1200mS/mm), and a significant increase of the input capacitance Cgs appears as expected. However, very good values close to 20 and 25 have been reached respectively for the Cgs/Cgd ratio and for the gm/gd voltage gain factor.
From S-parameters, the maximum stable gain MSG, the maximum available gain MAG and the current gain H_{21} have been calculated. On the Fig. 5 are illustrated the typical results obtained as a function of the frequency. The extrapolating extrinsic cutoff frequencies of current gain are 70GHz and 95GHz, respectively for the dual and single gate devices. If the cascode configuration exhibits as expected the highest MSG, up to 110GHz, the frequency

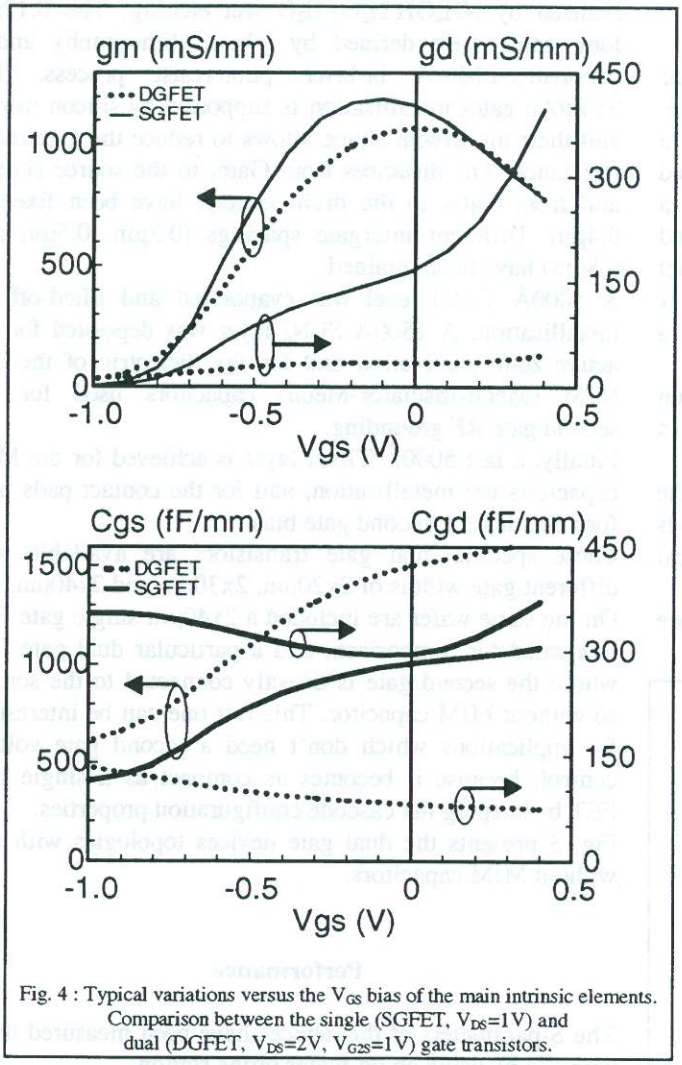

Fig. 4 : Typical variations versus the V_{GS} bias of the main intrinsic elements. Comparison between the single (SGFET, V_{DS}=1V) and dual (DGFET, V_{DS}=2V, V_{G2S}=1V) gate transistors.

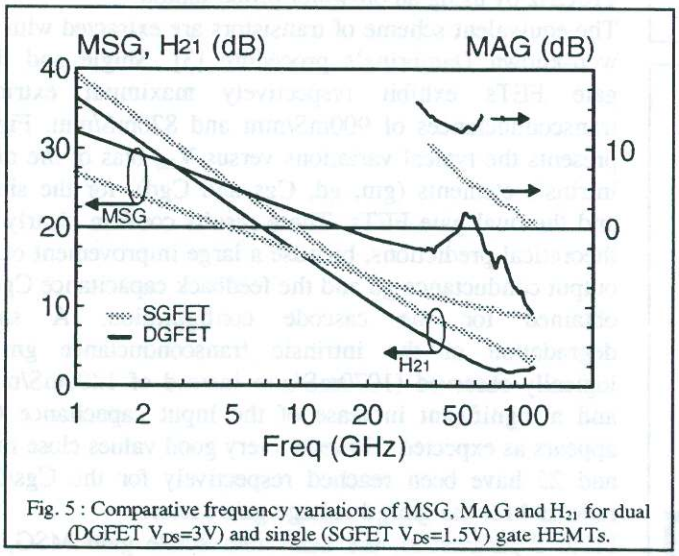

Fig. 5 : Comparative frequency variations of MSG, MAG and H_{21} for dual (DGFET V_{DS}=3V) and single (SGFET V_{DS}=1.5V) gate HEMTs.

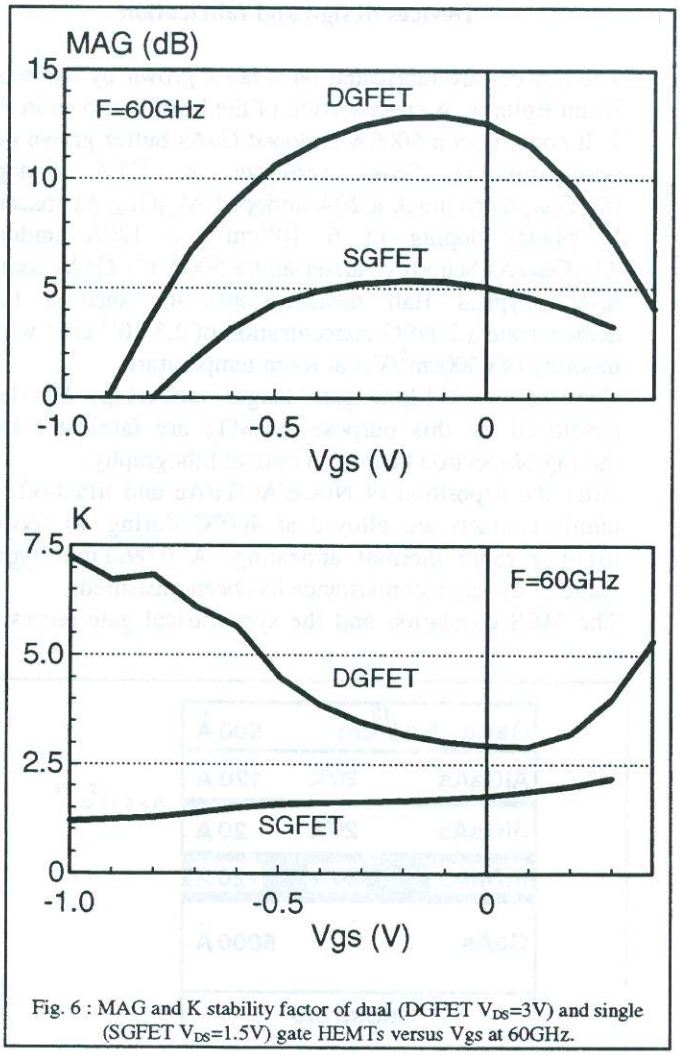

Fig. 6 : MAG and K stability factor of dual (DGFET V_{DS}=3V) and single (SGFET V_{DS}=1.5V) gate HEMTs versus Vgs at 60GHz.

variation of this gain is different and particularly in the millimeter wave range. Indeed a large resonance occurs at about 60GHz, that leads to values clearly higher than 20dB. This frequency resonance seems to depend strongly on the gate width, because it appears systematically at 40GHz, 60GHz and 80GHz respectively for the 2*40µm, 2*30µm and 2*20µm dual gate transistors, with or without the MIM capacitors. In fact, it is the parasitic access inductance of the second gate, which is responsible of this resonance effect. Electrical simulations have confirmed these results by using the complete equivalent scheme of dual gate devices [4].

Moreover, the stability conditions are not affected by this resonance phenomenon. Fig. 6 presents the variations of the maximum available gain and the K stability factor, versus the V_{GS} bias, for the 2*30µm dual gate and the single gate devices at 60GHz. The great advantage of the cascode configuration is demonstrated, because we obtain a MAG whose the maximum value is higher of about 8dB than the single gate one's, with a peak value of 13dB. Then, according to the K factor really greater than the unity, the dual gate transistors points out a very good unconditionally stability.

On wafer noise parameters measurements have been performed in the frequency range from 6GHz to 19GHz, at 60GHz and at 94GHz, by using a method developed in our laboratory [5,6]. Fig. 7 presents the frequency dependences of the minimum noise figure NFmin and the associated gain Gass, for the single and dual gate transistors, up to 19GHz. If the noise figures are similar in the both cases, we still measure better characteristics for the cascode configuration in term of associated gain. A very low noise

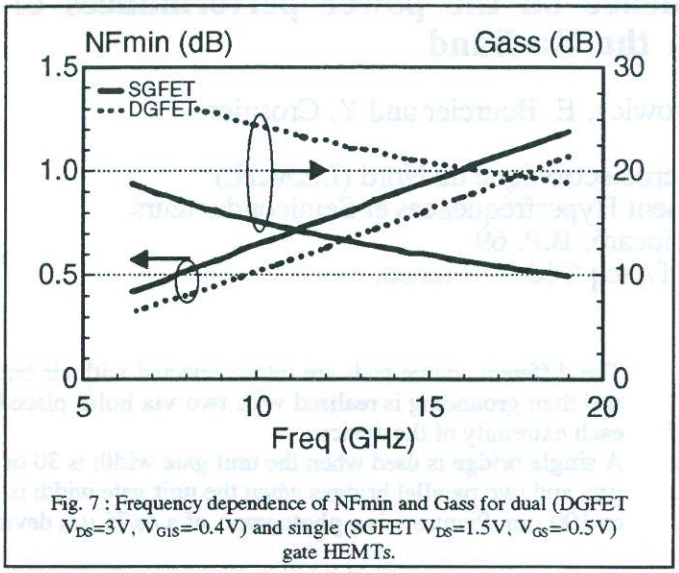

Fig. 7 : Frequency dependence of NFmin and Gass for dual (DGFET V_{DS}=3V, V_{GIS}=-0.4V) and single (SGFET V_{DS}=1.5V, V_{GS}=-0.5V) gate HEMTs.

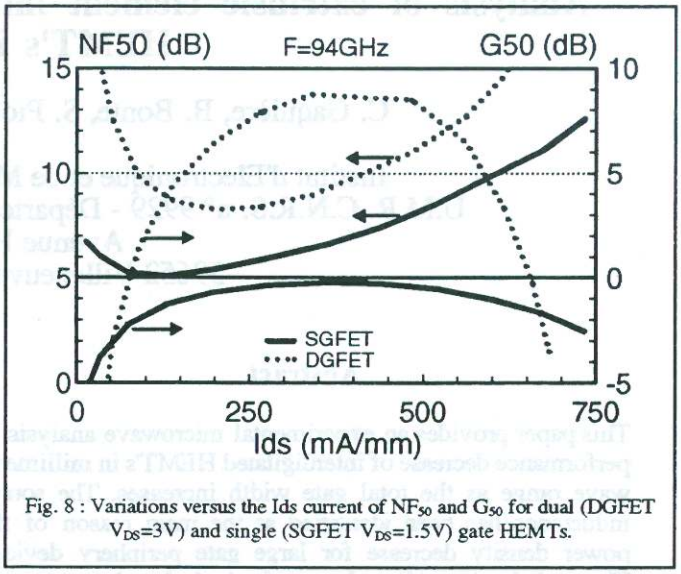

Fig. 8 : Variations versus the Ids current of NF_{50} and G_{50} for dual (DGFET V_{DS}=3V) and single (SGFET V_{DS}=1.5V) gate HEMTs.

figure of 1dB is obtained at 18GHz with Gass=20dB, instead of 10 dB for the SGFET. NFmin falls down to 0.5 dB with Gass=24dB at 10GHz for the DGFET.

We report the noise figure NF_{50} and the associated gain G_{50} measured at 94GHz versus the Ids current (Fig. 8). NF_{50} represents the noise figure in the case of 50Ω source impedance. It appears that in the millimeter wave range the dual gate device becomes noisier than the SGFET (minimum NF_{50} of 8dB instead of 5dB). This can be explained by the fact that the more the frequency increases, the more the first common source stage's gain of the cascode configuration decreases, and so, the noise contribution of the second common gate stage becomes more and more important. In low frequency, the gain of the first stage is large enough to muffle this effect, it is the reason why both single and dual gate FETs noise figures are equivalent.

On the other hand, the maximum associated gain G_{50} of the dual gate transistor remains close to 9dB at 94GHz, while the SGFET's one does not exceed 0dB.

Conclusion

Single and dual 0.12µm AlGaAs/InGaAs/GaAs pseudomorphic HEMTs have been designed, realized and characterized. The presence of the second gate clearly improves the output conductance gd, which tends to become too high with ultra-short gate FETs, and it reduces significantly the feedback capacitances Cgd.

Extremely high gains up to 110GHz and good noise figures have been measured for the dual gate transistors used in cascode configuration, well suited for the low noise amplification in the millimeter wave range.

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